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Nonvolatile memory with graphene oxide as a charge storage node in nanowire field-effect transistors

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Through the structural modification of a three-dimensional silicon nanowire field-effect transistor, i.e., a double-gate FinFET, a structural platform was developed which allowed for us to utilize graphene oxide (GO) as a charge trapping layer in a nonvolatile memory device. By creating a nanogap between the gate and the channel, GO was embedded after the complete device fabrication. By applying a proper gate voltage, charge trapping, and de-trapping within the GO was enabled and resulted in large threshold voltage shifts. The employment of GO with FinFET in our work suggests that graphitic materials can potentially play a significant role for future nanoelectronic applications.
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Owing to its role as a precursor to graphene, graphene oxide (GO) has attracted substantial interests from the scientific community.[1] Recently, various studies have been carried out to find different ways to utilize GO. These efforts include using GO as a channel region in thin film transistors (TFTs),[2] testing the potential of GO as a dielectric material in organic field-effect transistors (OFETs),[3] and employing GO in memory applications.[4,5] The structure of a GO is known to consist of a hexagonal ring-based carbon network with sp^2-hybridized carbon atoms and sp^3-hybridized carbons bearing hydroxyl and epoxide functional groups on either side of the sheet, while the edge area of the GO contains carboxyl and carbonyl groups.[6,7] Within the GO, the oxygen functionalities and the defects that originate from the chemical structure of the edge area can act as a charge trapping site.[8] With the ample space it provides for charge trapping, several research groups have investigated GO for its role in a nonvolatile memory device.[9,10] As much as the abundant charge trapping capacity GO contains is interesting, due to the weak immunity GO has against temperature,[9] it is highly difficult to realize a nonvolatile memory device with GO on a complementary metal-oxide semiconductor (CMOS)-compatible FET as the properties of GO would severely alter during the fabrication steps. Moreover, for planar FETs and organic FETs, when the device is realized on the silicon-on-insulator (SOI) substrate, as the silicon substrate acts as a global backgate, the device lacks individual addressibility. For memory operations, monolithic integration with an external circuit is crucial for practicality.

To address the above issue, herein, we report a structural platform derived from a FinFET, which enabled us to develop a CMOS-compatible nonvolatile memory using GO as the charge trapping site. The top-down approach utilized in our work is exceptionally simple, precisely controllable, and easily reproducible. Furthermore, as a viable candidate for developing future computer chips, FinFETs have recently been announced in the media for commercialization due to the smaller device size and stronger immunity against short-channel effect that FinFETs have compared with planar FETs.[11,12]

The overall configuration of the proposed device is illustrated in Fig. 1(a). An n-channel double-gate FinFET, in which the silicon fin is sandwiched between the two gate electrodes, was modified for the realization of the proposed device. That is, to provide a space for the injection of the aqueous GO, the gate oxide was replaced with an air gap. Through sufficient etching, the gate oxide was completely removed, and subsequently 3 nm of silicon dioxides were regrown on the exposed surfaces of both the channel and the gates through thermal oxidation in the furnace for 30 min at 700 °C. For planar FETs, due to structural limitations, the fabrication process requires thermal annealing of the source and drain after the insertion of the GO. As a result, much of the electrical properties of GO are altered, and the charge trapping capacity is reduced.[9,13] In that sense, the particular structure of the proposed device is highly advantageous as it can allow for the introduction of the GO after all the high temperature fabrication steps have been carried out including annealing which is required for improving transistor characteristics.

The process of inserting GO was simple because, as previously reported, GO is soluble in many different solvents and can be uniformly deposited onto a wide range of substrates.[14] To attach the GO material, 3-aminopropyltriethoxysilane (APTES), which serves as an adhesion layer, was coated on the device prior to the introduction of the GO. By dipping the device in a solution containing aqueous APTES solution mixed with de-ionized water in 1:100 ratio for 30 min, the coating of the APTES was completed. Then, by dipping the same device in an aqueous GO solution for 30 min, GO was attached to the channel and the gate area. As a result, we were able to obtain a final structure in which the GO is located between the gates and the channel, and the regrown oxides enclosing the GO served as the tunneling and blocking oxides for the memory operation.

The GO used in this work was acquired from following a modified Hummer's method.[15] Figure 1(c) shows the Raman spectrum of the GO that was used for this work. The first peak at the frequency of 1335 cm^{-1} corresponds to

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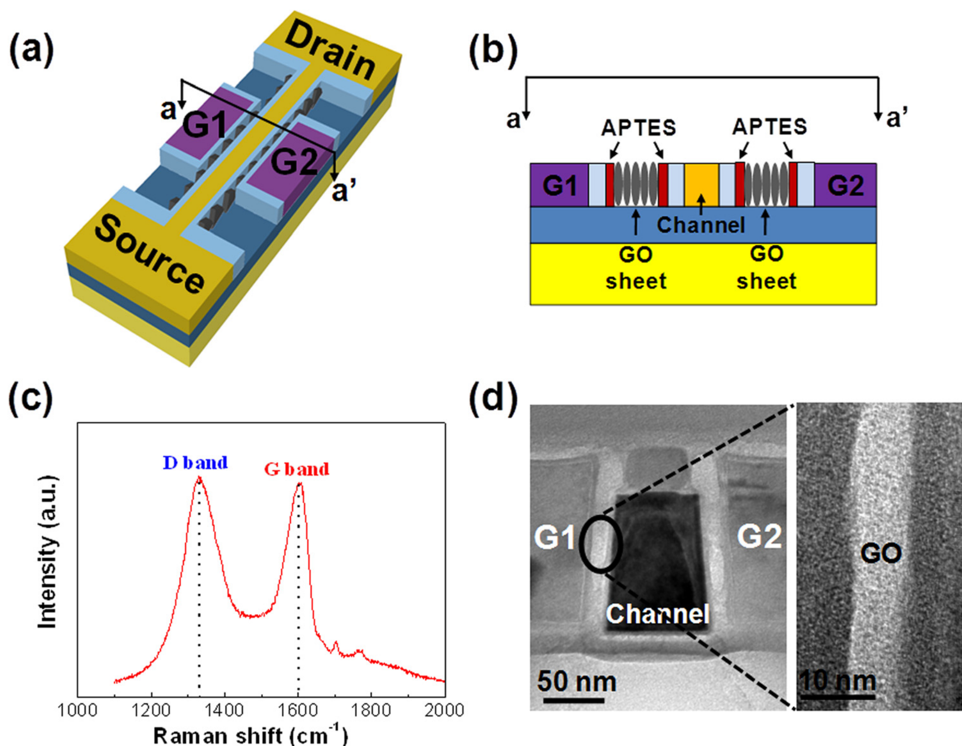

FIG. 1. (Color online) (a) Schematic illustration of the proposed device with the GO embedded. The final configuration is formed by an initial gate oxide removal from the double-gate FinFET, followed by a slight re-oxidation, and finally the introduction of the GO material. Due to the initial removal of the gate oxide, a nanogap is formed in which the GO can enter into. (b) Cross-sectional schematic of the final GO-embedded device. (c) Raman spectrum of the GO used for the characterization. (d) Cross-sectional transmission electron microscopy (TEM) image of the GO-embedded device with a close-up view of the region between the channel and the gate.

the D band while the second peak at 1600 cm^{-1} corresponds to the G band. Conventionally, the intensity ratio I_D/I_G of the two peaks is widely used for characterizing the defect quantity within the graphitic materials.[16,17] By controlling the amount of defect quantity, the electronic and mechanical properties of the GO can be tuned to the user's purpose.[18] Thus, the trapping sites within the GO and therefore the amount of threshold voltage shift can be readily modulated. In our case, in order to provide an abundant room for charge storage, it was desirable to have a more severely fragmented GO. We imagine that as the device scales down, the uniformity of the GO material with respect to both its size and fragmentation will be increasingly important for obtaining reliable memory characteristics. The obtained GO was embedded within the fabricated device and the cross-sectional view of the finalized structure is as presented in Fig. 1(d). Here, it should be noted that the thicknesses of the oxides adjacent to the gate and the channel are about the same. In order to confirm the presence of the GO within the nanogap after its insertion, an elemental mapping was performed with the energy dispersive spectroscopy (EDS). The mapping for silicon in Fig. 2(a) results from the polysilicon gates and the silicon channel, while that of the nitrogen element shown in Fig. 2(d) is from the hard mask and the passivation layer. As illustrated in Figs. 2(b) and 2(c), the oxygen and carbon atoms show high intensity signals concentrated at the nanogap region. The carbon element is relatively less clear compared with other elements as carbon is more vulnerable to the surrounding noise. Knowing that GO consists of both oxygen and carbon, the EDS mapping clearly supports the attachment of GO on the channel and the gates. Furthermore, due to the presence of the regrown oxide layers, oxygen shows a more apparent pattern compared with carbon.

To study the charge trapping properties of the GO, the current-gate voltage (I-V_G) hysteresis was measured from n-channel devices with a gate length of 1 μm and nanowire width ranging from 40 to 60 nm. The obtained I-V_G curve was then converted to a conductance-gate voltage (G-V_G) curve by the relationship $G = I/V_{ds}$, where V_{ds} is the drain-source voltage. As illustrated in Fig. 3(a), for the GO embedded device, it was found that the ratio between the high conductance on state and the low conductance off state was as large as 10^7. After the initial read, the device was switched to an erased state by applying +10 V. When a positive voltage was applied to the gates, the threshold voltage (V_T) shifted in a leftward direction and the device was turned on

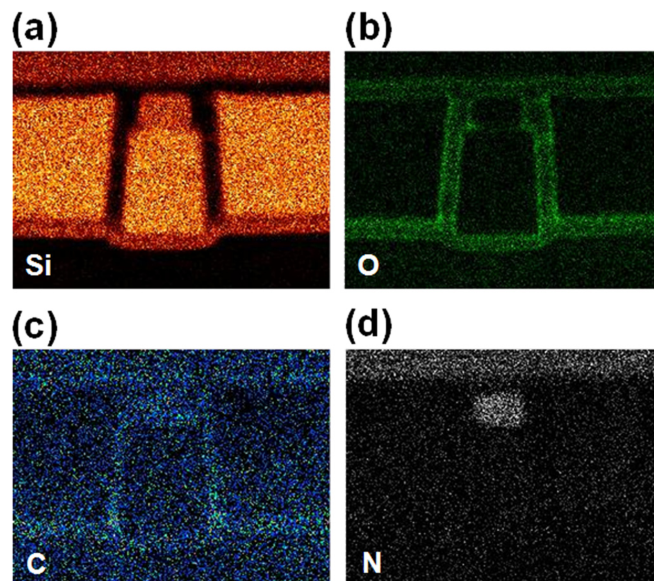

FIG. 2. (Color online) Analysis of the gap region between the gates and the channel for a GO-embedded device. Elemental mapping with EDS for (a) silicon, (b) oxygen, (c) carbon, and (d) nitrogen.

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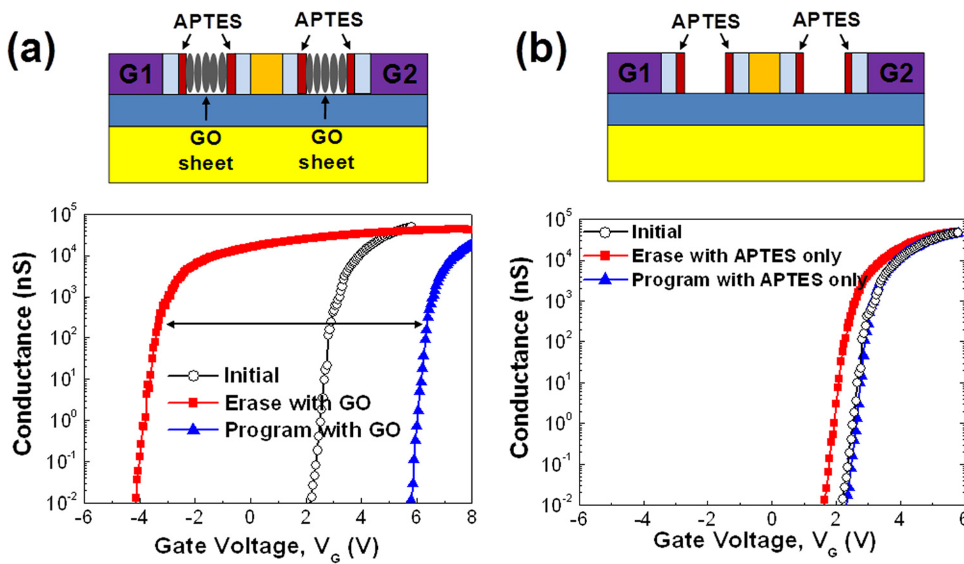

FIG. 3. (Color online) (a) G versus V_G for the final GO-embedded device with 0.05 V of V_{ds} applied. The initial curve (black) shifts to the right (blue) as a V_G of −10 V is applied. The converse is true when a V_G of +10 V is applied. The right curve (blue) shifts to the far left (red). The double-headed arrow indicates the wide memory window between the "programmed" and "erased" states. (b) G versus V_G with only the APTES adhesion layer attached to the gate and the channel. Without GO, the hysteresis is greatly reduced.

at a lower voltage. Designating 2000 nS to be the high conductance on state, which corresponds to a drain current of 10^{-7} A when 0.05 V of V_{ds} is applied, the V_T shifted by 6.05 V after the erase. From the erased state, when a subsequent V_G of −10 V was applied, the device switched to a programmed state and the V_T shifted rightward by 9.45 V. To confirm that the APTES layer was not a factor for the large hysteresis, a control experiment with only the APTES layer was carried out. As illustrated in Fig. 3(b), the hysteresis is markedly small, implying that the GO clearly functions as a charge trapping site. As illustrated in Fig. 4(a), when a negative V_G is applied (e.g., program operation), electrons from the heavily doped n-type polysilicon gate tunnel through the oxide layer and are stored in the traps within the GO. Due to the lower mobility and higher potential barrier experienced by the holes compared with that of the electrons, electrons play a dominant role during the tunneling process. As the electrons are trapped within the GO, larger V_G is required for the creation of an inversion layer in the channel and thus the V_T is increased. As positive V_G is applied, the electrons within the GO layer tunnel back into the gate, and thus smaller V_G is necessary for the channel inversion. To confirm that the mechanism behind the program and erase involves tunneling, control experiments were performed for three different tunneling oxide thicknesses (T_{OX}). For the three different T_{OX}, that is, 3, 5, and 7 nm, the following oxidation conditions were employed: 700 °C for 30 min, 750 °C for 30 min, and 750 °C for 45 min. As presented in Fig. 4(b), as T_{OX} was increased, less hysteresis was shown. As widely known, the tunneling probability of the electrons decreases greatly for increased T_{OX}. Hence, when T_{OX} is increased, smaller number of electrons would travel into the GO region and would result in reduced number of trapped electrons within the GO.

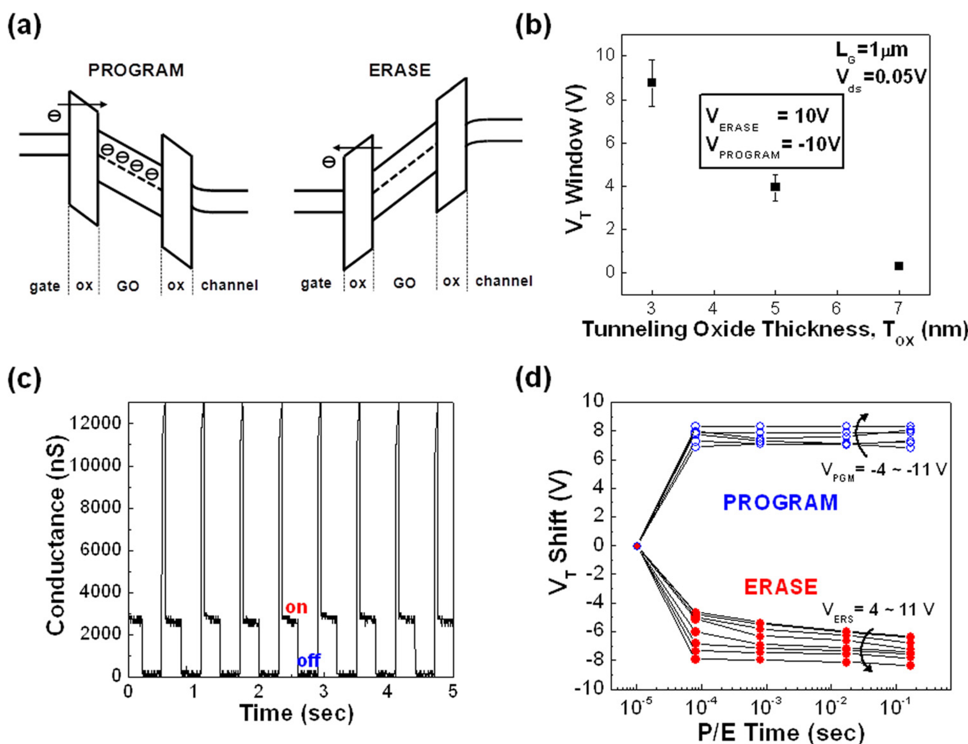

FIG. 4. (Color online) (a) Operation of program and erase. (b) Amount of V_T shift for different T_{OX}. (c) *On* and *off* switching of the device using +10 V and −10 V. During erase and program, V_G of +10 V and −10 V, each with a pulse width of 50 ms were employed, respectively. The *on*/*off* states were read with a V_G of 2 V and a V_{ds} of 0.05 V for 250 ms. Hence, the total period of a single cycle was 0.6 s. (d) *Program*/*Erase* time versus V_T shift with different V_G applied for both program and erase.

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We extended our study by measuring the on/off cycles. Our device showed excellent endurance as the switching between on and off states maintained the same conductance change for at least 10^4 cycles and the typical on/off cycles are as shown in Fig. 4(c). Moreover, large hysteresis was observed even for small V_G applied. The V_T shifts for different V_G applied are shown in Fig. 4(d). As the magnitude of the applied V_G is increased, the amount of hysteresis is increased as well. It should be noted that in Fig. 4(d), the V_T shift for program and erase each represent hysteresis from its counter state. For the erased state, as the erase time and the magnitude of the applied V_G is increased, the hysteresis is increased as well. However, for the programmed state, though the increased magnitude of the applied V_G resulted in larger hysteresis, the program time did not have a significant influence. During program, as electrons are simply being tunneled into the GO layer, the operation occurs quickly and a large hysteresis can occur at a relatively short amount of time. However, during erase, as the trapped electrons must be de-trapped before the tunneling, the time seems to play a bigger role.

Finally, the retention time of the proposed device have been characterized. Figures 5(a) and 5(b) represent the retention time for different T_{OX}, 3 and 5 nm, respectively. For 3 nm of T_{OX}, though the initial on/off ratio of the conductance between the erased and programmed states was 10^6, the large ratio was reduced to a difference of only one order in a relatively short period of time (<1000 s). On the other hand, when the T_{OX} was increased to 5 nm, though the initial on/off ratio was decreased to 10^3, the gap between the two states remained for an increased period of time. Thus, by optimizing the T_{OX} to fit our purpose, we can either obtain excellent retention time or large on/off ratio. We believe the variability of the retention time is likely due to the variations in the electron tunneling probability. Moreover, the characteristics of the GO material itself may influence the retention time. As well-known, the main transport mechanism within GO is lateral conduction which occurs by hopping between localized states.[19] Thus, reduced GO can possibly worsen the retention by increasing the density of such localized states[20] and charge leakage.

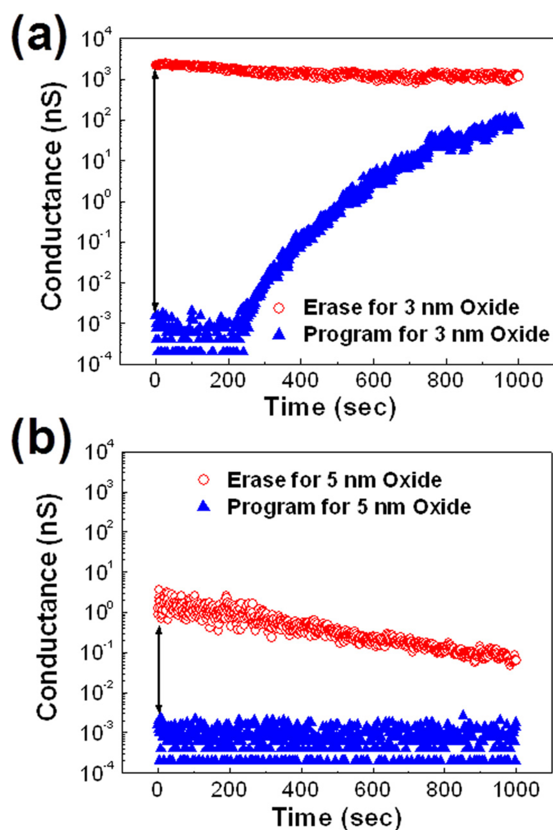

FIG. 5. (Color online) Retention characteristics of the GO-embedded device with T_{OX} of (a) 3 nm and (b) 5 nm. The upper and lower curves stand for erased and programmed states, respectively.

In summary, to study the charge trapping properties of GO without altering its innate characteristics, a FinFET was modified for the realization of a structure that can allow for the insertion of the GO after the complete fabrication of the device. As the proposed device is directly derived from a FinFET, it is CMOS-compatible, individually addressable, and extremely practical. More importantly, due to GO's large charge trapping capacity, memory window was shown to be as wide as 9.45 V. Together with the solution-processability of GO and the unique structure of the proposed device, we were able to obtain results that demonstrate the potential usage of graphitic materials with respect to the silicon technology.

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