Combined Image Signal Processing for CMOS Image Sensors

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Abstract

This paper presents an efficient image signal processing structure for CMOS image sensors to achieve low area and power consumption. Although CMOS image sensors (CISs) have various benefits compared with charge-coupled devices (CCDs), the images obtained from CISs have much lower quality than those from CCDs. To improve the quality of CIS images, it is required to do reproducing and enhancing processings such as color interpolation, white balancing, color correction, gamma correction and color conversion. They are implemented individually in most conventional designs though they have similar functional characteristics. In this proposed structure, the gamma correction block is moved to the front in order to combine several image signal processings into one block. An efficient compensation scheme is also proposed to reduce the errors caused by the moving of the non-linear gamma correction. A prototype CIS image signal processor is implemented in Verilog-HDL and synthesized with 0.18um standard cell library. Experimental results show that the proposed structure reduces area and power consumption by 23.8% and 31.1%, respectively.

I. INTRODUCTION

According to the recent requirements of multimedia applications, digital still and video cameras are rapidly becoming widespread. They are enabling many new applications such as PC cameras, digital cameras integrated into cell phones and PDAs, intelligent toys, and so on. Most imaging systems have used charge-coupled devices (CCDs) [1,2] to capture images because the image sensor plays a vital role in the quality of images. However, it is not easy for CCDs to be integrated with other functions. In addition, they are consuming high power.

As imaging systems are adopted primarily in mobile applications, area and power consumption are very decisive factors to be considered in their implementation. Thanks to the benefits of CMOS image sensors (CISs) [3,4], such as low cost, low power, and high integration, CISs are rapidly replacing CCD sensors. The image quality of CISs is, however, not as good as that of CCDs, and typical CISs provide only one color component per pixel. Therefore, CISs need lots of image signal processings to reproduce and enhance the quality of image.

In most conventional designs [5-7], the processings are implemented individually as shown in Fig. 1, because nonlinear operations are intervened between linear operations. However, some computations are so similar that they can be combined into a single computation if the nonlinear operations are relocated. To reduce not only hardware area but also power consumption, we proposed in this paper a new image signal processing structure that combines multiple processings into one block.

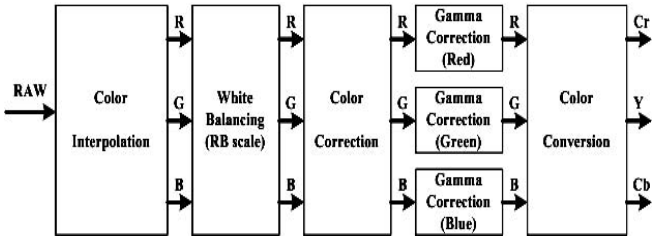

Figure 1. Conventional Image Signal Processing Structure

II. CONBINED IMAGE SIGNAL PROCESSING

Fig.1 depicts the block diagram of a conventional CIS image signal processor, which consists of several image signal-processing blocks to reproduce and enhance the quality of CIS image. Since a CIS usually employs a color filter array (CFA) to lower its cost [9], it provides only one component of RGB data per pixel. Therefore, color interpolation is necessary to reproduce the omitted color components. In the white balancing unit, the values of red and blue are scaled to make the images similar to what the human eyes perceive. The two scaling factors for red and blue are usually obtained by analyzing the intensity of the color components [10]. Since a display device has its own color space, color correction is required to transform the color space into another one corresponding to the display device [11], and gamma correction adjusts the image data so that the display device shows the intensity proportional to its input. Color conversion converts *RGB* color space into YC_bC_r space because the latter is more efficient for image compression and enhancement.

The operations of white balance, color correction and color conversion are linear and very similar to one another. These operations can be represented as matrix multiplications and combined into one matrix multiplication if the nonlinear gamma correction is relocated to another place as shown in equation (1):

$$\begin{pmatrix} CV_{CrR} & CV_{CrG} & CV_{CrB} \\ CV_{YR} & CV_{YG} & CV_{YB} \\ CV_{CbR} & CV_{CbG} & CV_{CbB} \end{pmatrix} \times \begin{pmatrix} CC_{RR} & CC_{RG} & CC_{RB} \\ CC_{GR} & CC_{GG} & CC_{GB} \\ CC_{BR} & CC_{BG} & CC_{BB} \end{pmatrix} \times \begin{pmatrix} WB_{red} & 0 & 1 \\ 0 & 1 & 0 \\ 0 & 0 & WB_{blue} \end{pmatrix} \quad (1)$$

where WB_{red} and WB_{blue} are scaling coefficients for white balancing and $\{CC_{ij}\}$ and $\{CV_{ij}\}$ are the matrices of converting coefficients for color correction and color conversion, respectively. First, color conversion and color correction operations can be merged into one matrix multiplication [*CVC*] as shown in (2). Actually, the coefficients should be programmable by users through the I^2C interface, as those of [*CV*] and [*CC*] are programmable.

$$\begin{pmatrix} CVC_{CrR} & CVC_{CrG} & CVC_{CrB} \\ CVC_{YR} & CVC_{YG} & CVC_{YB} \\ CVC_{CbR} & CVC_{CbG} & CVC_{CbB} \end{pmatrix} \times \begin{pmatrix} WB_{red} & 0 & 1 \\ 0 & 1 & 0 \\ 0 & 0 & WB_{blue} \end{pmatrix} \quad (2)$$

Then, the merged [*CVC*] and white balancing operation can be also combined into a combined matrix [*COM*] to reduce hardware area and power consumption as follows:

$$\begin{pmatrix} COM_{CrR} & COM_{CrG} & COM_{CrB} \\ COM_{YR} & COM_{YG} & COM_{YB} \\ COM_{CbR} & COM_{CbG} & COM_{CbB} \end{pmatrix} \quad (3)$$

In spite of this fact, they are implemented separately in conventional designs [3-5] because the gamma correction block is located between color correction and color conversion as shown in Fig. 1. To combine the three blocks, the gamma correction has to be moved to the front of the processing structure. However, as the gamma correction is not a linear function, it is hard to change its location without compensating the nonlinearity.

Fig. 2 shows the overall structure of the proposed CIS image signal processing, where three blocks of white balancing, color correction, and color conversion are combined into a single matrix multiplication block and an efficient compensation is employed in the color interpolation block.

In addition to this, there is another advantage in the proposed structure. Since the raw CIS data contains only one color component per pixel, one gamma correction block is sufficient to do the gamma correction for the raw CIS data. Therefore, the proposed structure requires only one gamma correction block, not three blocks as in the conventional design.

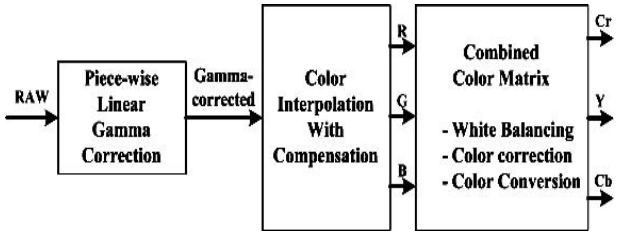

Figure 2. Proposed Image Signal Processing Structure

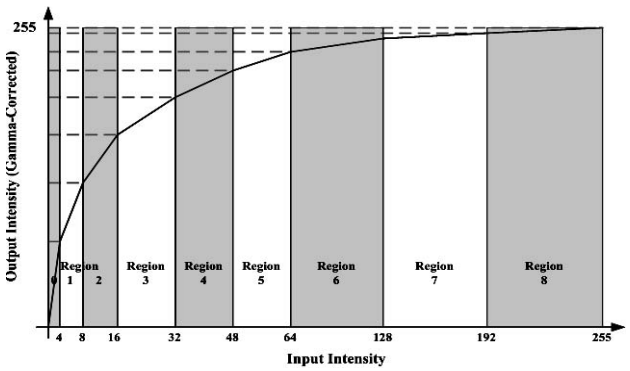

Figure 3. Piece-wise Linear Gamma Correction

III. EFFICIENT COMPENSATING SCHEME

In the proposed structure, color interpolation and gamma correction that are both nonlinear are combined into one block. Most image signal processors employ the bilinear interpolation algorithm for color interpolation [8]. The operations of the bilinear interpolation can be explained as follows. If we assume that *C*, $\{A_{ij}\}$ and $\{B_{ij}\}$ in Fig. 4 are the current calculated point and its neighbors, the $\{result_i\}$ in equations (4), (5) and (6) are the missing color components to be reproduced by applying the interpolation algorithm. As inferred from equations (4), (5) and (6), the interpolation operations can be considered as averaging of two neighbors or two averages of them.

$$result_A = \left\{ \left(A_{1a} + A_{1b} \right) / 2 + \left(A_{2a} + A_{2b} \right) / 2 \right\} / 2 \quad (4)$$

$$result_{B_1} = \left(B_{1a} + B_{1b} \right) / 2 \quad (5)$$

$$result_{B_2} = \left(B_{2a} + B_{2b} \right) / 2 \quad (6)$$

A_{1a}	B_{1a}	A_{1b}
B_{2a}	C	B_{2b}
A_{2a}	B_{1b}	A_{2b}

Figure 4. The pairs of neighbor in the bilinear interpolation

The nonlinear gamma function is usually approximated by a piece-wise linear function in practical implementations. We assume that the function has 9 piece-wise linear regions, i.e., from region 0 to region 8, as shown in Fig. 3. An enlarged part of the gamma correction function is shown in Fig.5. It is linear in a region, but it still suffers from the nonlinear distortion near the region boundaries. Let us consider two inputs, *a* and *b* of the gamma function $G(x)$.

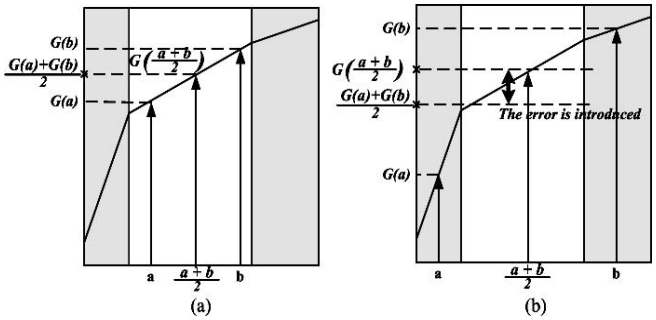

Figure 5. Exmaples of Two inputs
(a) Two inputs in the same region (b) Two inputs in different regions

The result of color interpolation and gamma correction in the conventional structure can be represented as equation (7). In the other hand, the proposed structure calculates the result as equation (8) since the gamma correction block is located prior to the color interpolation block. Therefore, a significant distortion can be introduced when the missing color components are recovered using the color interpolation.

$$G\left((a+b)/2\right) \tag{7}$$

$$\left\{G(a)+G(b)\right\}/2 \tag{8}$$

We have observed how much error is resulted from moving the gamma correction block to the front. There are two cases to be considered as shown in Fig. 5; one is when two inputs are in the same region of gamma function, another when two inputs are in different regions. Since the gamma function is piece-wise linear in a region, the color interpolation introduces no difference as shown in Fig. 5(a) when two inputs are in the same linear region although the gamma correction block is moved toward the front. As shown in Fig. 5(b), if two inputs are not in the same region, however, the difference is not avoidable due to the non-linearity at the region boundaries, leading to large image distortion. Therefore, we have observed the average differences when two inputs are in different linear regions.

TABLE I. SUMMARY OF ROOT MEAN SQUARE ERROR

RMSE		Region of Input a								
		8	*7*	*6*	*5*	*4*	*3*	*2*	*1*	*0*
Region of Input b	*0*	46.89	39.39	33.48	24.21	20.21	15.16	10.75	5.32	-
	1	33.34	25.71	20.40	12.13	8.06	4.49	1.90	-	
	2	27.01	19.23	14.76	7.31	4.29	1.98	-		
	3	19.87	12.01	8.66	3.14	1.69	-			
	4	13.88	6.47	3.87	1.18	-				
	5	9.93	3.49	1.09	-					
	6	5.98	1.98	-						
	7	1.46	-							
	8	-								

TABLE II. COMPENSATION OFFSETS

Distance	Compensating Offset	
	Region 0 included	*Otherwise*
1	5	2
2	10	4
3	15	8
4	20	13
5	24	20
6	33	26
7	39	33
8	46	

Table I summaries the difference according to the distance of regions to which the two inputs belong. If one input is included in region 0 of Fig. 3, the difference is larger than any other cases, as indicated in the first row of Table I.

The proposed compensation scheme is to add an approximate offset to the color interpolation operation. First, we determine what regions two inputs are in and calculate the distance between the two regions. According to the distance, the compensator selects one of the offsets shown in Table II. To take into account the case that one input is in region 0, two offsets are provided for a distance. The offset values and the region boundaries are determined to minimize the difference as much as possible by taking into account hardware complexity. Finally, the selected offset is added to the result of color interpolation operation. By adding the compensation offset, we can significantly reduce the error caused by the relocated gamma correction block.

IV. EXPERIMENTAL AND SYNTHESIS RESULTS

The combined image signal processing is modeled in C-language and simulated for several practical images. The image quality is compared to the conventional separated processing as summarized in Table III. The performance difference is only 1.03dB in terms of PSNR on the average, and the difference is not perceptible for all the images we have tested as shown in Fig. 7.

To compare area and power consumption with the conventional design, a prototype CIS image signal processor is implemented in Verilog-HDL and synthesized with a

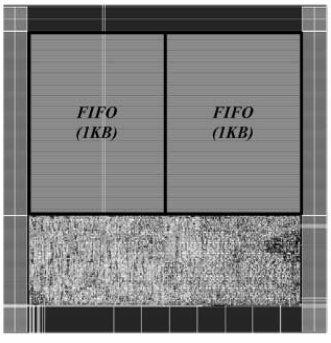

Figure 6. Layout of Proposed Image Signal Processor

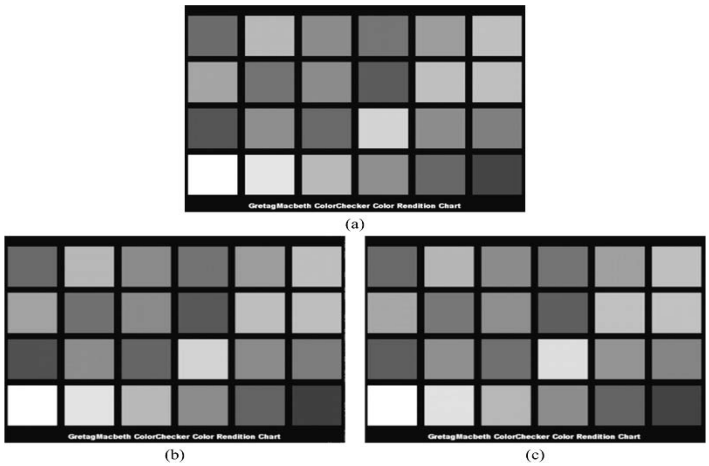

Figure 7. Examples of Experimental results (a) Original image (b) Conventional processings (c) Proposed processings

CMOS 0.18um standard cell library. The layout shown in Fig. 6 occupies 0.76mm × 0.76mm including two FIFO memories.

Table III also compares the area in terms of the equivalent gate count and power consumption at 50MHz. Compared with the conventional design, the area and power consumption are reduced by 23.8% and 31.1%, respectively.

TABLE III. EXPERIMENTAL AND SYNTHESIS RESULTS

Design	Performance (PSNR, dB)	Area (gate counts)	Power (mW @ 50MHz)
Conventional	**28.02**	**26.823**	**26.19**
Proposed	**26.99**	**20.454**	**18.03**
Comparisons	**1.03 (3.7%)**	**23.8%**	**31.1%**

V. CONCLUSION

In this paper, we have presented an efficient image signal processing structure for CMOS image sensors. In order to achieve low area and power consumption, the proposed structure combines several computation blocks into one block. By moving the gamma correction block toward the front, three blocks for white balancing, color correction, and color conversion can be combined into a single block. In addition, the gamma correction operation is reduced to only one block, not three blocks as in conventional designs. Employing an effectual compensation scheme in the color interpolation operation reduces the non-linearity error caused by moving the gamma correction. As a result, the combined image signal processing significantly reduces hardware area and power consumption without perceptible performance degradation.

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