Characteristics of silicon nanocrystal floating gate memory using amorphous carbon/SiO₂ tunnel barrier

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Nanocrystal floating gate memory employing an amorphous carbon (a-C)/SiO₂ double-layered tunnel barrier was fabricated. The band gap of a-C and conduction band discontinuity between a-C and Si was estimated to be 1.95 and 0.4 eV, respectively. In addition, interface states density of the a-C/SiO₂/channel Si was estimated from the capacitance–voltage measurement. The nanocrystal memory using this tunnel barrier exhibited enhanced charge retention than that employing a single SiO₂ tunnel barrier whereas the injection efficiency is comparable between them, which is due to the asymmetrical band profile of the tunnel barrier. © 2002 American Institute of Physics.

Nanocrystal floating gate memory (NFM) is a candidate for one of the future scaled flash memories. Moreover, it is faster, consumes lower power, and has complementary metal–oxide–semiconductor (CMOS) process compatibility. The primary advantage of this memory structure is employment of ultrathin tunnel oxide. However, to meet the trade-off between the speed and charge retention, proper profiling of the tunnel barrier structure is very critical.

It was pointed out that an asymmetrical tunnel barrier has a useful application area such as single electron circuits and nonvolatile memories. Upon this concept, it is possible to profile the tunnel barrier of NFM for the purpose of enhancing the charge retention without degradation in the injection efficiency. In fact, application of tunneling oxide/nitride in NFM was already reported, however, they did not point out the asymmetrical nature of the tunnel barrier. In this letter, we propose a tunnel barrier structure that is composed of amorphous carbon (a-C) and SiO₂ to attain enhanced charge retention without degradation in the injection efficiency.

The deposition of ultrathin a-C as well as nanocrystal array was performed using photochemical vapor deposition method (photo-CVD), because photo-CVD is known to have fine thickness controllability in nanometer scale. 2-nm-thick SiO₂ film was grown by oxidation at 400 °C under ultraviolet light irradiation, followed by 1.3-nm-thick a-C film deposition using the photo-CVD. Nanocrystal array was also deposited by the photo-CVD under the following conditions: temperature = 150 °C, pressure = 0.55 Torr, flow rate of SiH₄ = 1.3 sccm, and that of H₂ = 19.6 sccm. The estimated dot size was 10 nm width and 5 nm height, and the dot density was 3 × 10¹¹ cm⁻². Several structural parameters are indicated in the schematic illustration of the device structure shown in Fig. 1. For comparison, the NFM with only a single 2-nm-thick SiO₂ tunneling layer was also fabricated. Nanocrystal array grown on SiO₂ under the same condition as before has much denser distribution than that on a-C, and the dot size was estimated to be 3 nm and the density was 2 × 10¹² cm⁻².

The capacitance–voltage (C–V) characteristic of the metal–oxide–carbon–oxide–Si (MOCOS) shown in Fig. 2 provides information concerning charging effect at the a-C film and its interfaces. The shape of the curve is independent of the sweep speed. The stretch-out observed in the curve of MOCOS represents the charging effect in the a-C layer and its interfaces. As the voltage increases beyond the channel inversion condition, the inversion charges tunnel into the a-C. In that case, electrons are trapped at localized states such as a-C midgap states or interface states; therefore the width of the channel depletion region is sustained as constant with increasing gate bias. The dynamic threshold voltage shift as the total amount of stretch-out is about 4.4 V, and this value provides the effective density of interface states as 5.6 × 10¹² cm⁻². Although there is significant charging at the a-C layer and its interfaces, this does not contribute to the threshold voltage shift of the transistor. From the hysteresis C–V and drain current–gate voltage measurements, negligible flatband voltage shift (less than 0.1 V) was observed, which implies that the majority of the charges trapped at the

FIG. 1. Schematic illustration of the device structure. Indicated structure dimensions are obtained by transmission electron microscopy and spectroscopic ellipsometry measurement. 18 nm layer of SiO₂ was deposited at 470 °C by low pressure chemical vapor deposition.
$\alpha$-C layer and its interfaces easily tunnel back to the channel. The optical band gap was estimated to be 1.95 eV from the spectroscopic ellipsometry measurement.

Threshold voltage of the memory device with $\alpha$-C/SiO$_2$ (CO) tunnel barrier is plotted according to the programing voltage ($V_p$) at various pulse durations in Fig. 3(a). $V_p$ dependency on the threshold voltage shift reflects the injection efficiency versus bias voltage that can be approximated by a linear function in case of single tunnel barrier.\(^2\) In this plot, however, four curves commonly manifest a bump that can be explained by the characteristic of the tunneling probability. That is, the onset of the bump corresponds to the onset of the coincidence of the $\alpha$-C conduction band and the channel conduction band. From the simple calculation results demonstrated, Figs. 3(b) and 3(c) verify such a trend. Accordingly, the voltage value at the onset of bump ($V_{\text{bump}}$=4.5 V) implies the difference between the conduction band of the $\alpha$-C and the channel, which is 0.4 V. Consequently, the valence band discontinuity is extracted to be 0.45 eV by considering the band gap of $\alpha$-C (1.95 eV). The experimental data obtained from various $\alpha$-C films by Robertson identifies that the valence band discontinuity with Si ranges 0.4~0.1 eV,\(^{11}\) and Shafer obtained it for ultrathin $\alpha$-C (∼1.8 nm) as 0.3 eV.\(^{12}\) Our value is in the reasonable range and it is close to the Shafer’s for ultrathin $\alpha$-C.

The injection efficiency is higher for the device using a single tunnel barrier as shown in Fig. 4(a). At the same voltage drop at the tunneling layer ($V_{\text{bump}}$), the write time is about one order higher for the CO. The difference in the threshold voltage shift is relatively low for small $V_{\text{bump}}$ and increase around $V_{\text{bump}}$=0.6 V and decrease again at higher $V_{\text{bump}}$. This implies that the injection of electrons for the device using this CO tunnel barrier is only through the single barrier at high programming voltage (marked as “2” in Fig. 3). When scaling the $V_{\text{bump}}$ of the single tunneling barrier case (SB) by 1.5 times (the ratio of electrical thicknesses), the injection efficiencies for two different devices are almost similar at voltages higher than $V_{\text{bump}}$ as shown in Fig. 4(b). With the same pulse duration, as higher $V_{\text{bump}}$ as the electrical thickness ratio is required for the CO case to obtain the same threshold voltage shift. The threshold voltage observation versus time at zero bias condition shown in Fig. 5 presents the significant improvement of charge retention in the device using the CO tunnel barrier. In fact, this result was naturally anticipated from the fact that the tunneling discharge current exponentially decreases with the barrier width.

When profiling the tunnel barrier for enhancing the charge retention, the consideration of the injection efficiency is also important, because high injection efficiency and long charge retention are usually incompatible in memory devices. One of the main design issues may be the band alignment of the smaller band gap material relative to the channel Si. In our experiment, it was about 0.4 eV for electrons. Definitely, smaller values may not be helpful for the charge retention, and larger values may require higher programming voltage. Although the optimal value has not been investigated at this time, the $\alpha$-C/SiO$_2$ structure is appropriate for this purpose.

Diamond-like carbon may have compositional nonuniformity,\(^{13}\) which means variation in barrier height of $\alpha$-C layer in this device. In terms of the retention character-
istics, this variation only slightly affects the device. Even if the range of the variation is seriously large, the charge retention is not wholly degraded because the charge in dots on $\alpha$-C at which the band gap is over the average is retained as expected. This variation resistant characteristic is thought to be another benefit of this local charge storage device.

In conclusion, $\alpha$-C/SiO$_2$ tunneling layer was proposed for enhanced retention characteristic of the NFM. The deposited $\alpha$-C film has estimated band gap about 1.9 eV and conduction band discontinuity with Si about 0.4 eV. In addition, interface states density of the $\alpha$-C/SiO$_2$/channel Si was estimated from the capacitance–voltage measurement and also from the threshold voltage shift under various gate bias conditions. The NFM using this tunnel barrier exhibits enhanced charge retention than that employing a single SiO$_2$ tunnel barrier whereas the injection efficiency is comparable between them when additional write voltage is applied corresponding to the thickness ratio: thickness of total tunneling layer divided by thickness of SiO$_2$.


FIG. 4. (a) Normalized $V_T$ vs voltage drop at tunneling layer ($V_{tl}$) at various pulse durations for comparison between the device using SB and that using $\alpha$-C/SiO$_2$ tunnel barrier (CO). (b) Replotted version of (a) by multiplying the $V_{tl}$ of SB by 1.5.

FIG. 5. $V_T$ vs time at zero bias after programing with 4 V for 1 ms.