Physical Insights on Design and Modeling of Nanoscale FinFETs

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Abstract

An array of measured device data, a numerical device simulator, and a process/physics-based compact model are used to gain new and important physical insights on nanoscale FinFETs with undoped thin-fin bodies. The insights, which include unavoidable/needed gate underlap, bias-dependent effective channel length, and non-ohmic fin-extension voltage drops, reveal the significance of gate positioning on, and source/drain doping profile in, the thin fin, and imply novel compact modeling that will be needed for optimal design of nonclassical CMOS circuits.

Introduction

As the scaling of classical (i.e., bulk-Si and PD/SOI) CMOS is approaching a palpable limit, nonclassical MOSFET structures having ultra-thin Si bodies which facilitate scaling, including multiple-gate devices [1], [2], are being earnestly examined. The FinFET [3], [4], a quasi-planar double-gate (DG) transistor, is attracting much attention now because it is relatively easy to fabricate. The gate structure (of length L_g) of the FinFET, illustrated in Fig. 1, is "wrapped" over a thin Si fin (of thickness t_{Si}), yielding two active vertical gates that are beneficially charge-coupled [5] if t_{Si} is sufficiently thin, a specification, relative to the effective channel length (L_{eff}), which also ensures good control of short-channel effects (SCEs). The gate is necessarily separated from the source/drain (S/D) contact regions by extensions of the thin Si fin, features which complicate the design and modeling of the device as we reveal herein.

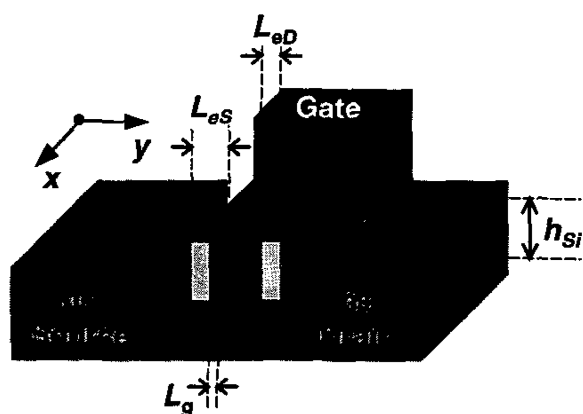

Fig. 1. The n-channel DG FinFET structure, with indications (L_{eS} and L_{eD}) of the undoped portions of the S/D fin extensions which are technologically unavoidable when the body of the nanoscale device is undoped. The gate for the nFinFETs studied herein [4] is n^+ polysilicon, and the gate insulator is nitrided oxide with physical thickness $t_{ox} = 1.7$nm.

Insights

The height (h_{Si}) of the Si fin, which is the effective gate width of the DG FinFET, is technologically limited to be not much larger than t_{Si}. Hence, the volume of the Si-channel region under the gate (i.e., $h_{Si}t_{Si}L_g$) of the nanoscale ($L_g < 50$nm) FinFET is small, which, technologically, tends to preclude the use of body doping for threshold control. (Metal gates with tuned work functions will probably be needed.) With undoped bodies and the implied low inherent doping density, the small FinFET body/channel will likely be virtually void of any dopants (i.e., *intrinsic*), and, because of technological limitations, so will portions (of lengths L_{eS} and L_{eD} as indicated in Fig. 1) of the S/D extensions adjacent to the gate. In fact, such a *gate-underlap* structure could be required to get optimal DG CMOS circuit speeds when $L_g < 25$nm [6]. Note that L_{eS} and L_{eD} are defined by the S/D lateral doping profile in the thin-fin extensions.

Consider L_{eff}, which can be thought of as the length over which the gate modulates the channel, or S-D conductivity; it governs SCEs as well as channel current (I_{ch}). For weak inversion, MEDICI [7] simulations of 2D cross-sections (x-y plane in Fig. 1) of nFinFETs show, in Figs. 2 and 3, that $L_{eff} > L_g$, i.e., that V_{GS} modulates the electric potential (ϕ) and the electron density (n) in the undoped fin-extension regions as well as in the channel. This modulation is a result of gate-induced electrons moving into the extensions and modifying the electric field to effect a perturbed drift-diffusion detailed balance in accord with I_{ch}. The modulation is governed, via Poisson's equation, by the Debye length, $L_D \propto 1/\sqrt{n}$. For weak inversion, n is low and L_D is relatively long (except near the S/D contact regions), implying

$$L_{eff(weak)} \cong L_g + L_{eS} + L_{eD} \quad , \qquad (1)$$

which is supported by the MEDICI results, including plots of $1/I_{ch}$ vs. L_g in Fig. 4. Further, as exemplified in Figs. 5-7, the long $L_{eff(weak)}$ in (1) is corroborated by calibrations of our process/physics-based model UFDG [8] to FinFETs that were fabricated using the process described in [4], in which the body/channel is left undoped and the S/D fin extensions are doped by 0°-tilt ion implantation with gate sidewall spacers, thereby yielding L_{eS}, $L_{eD} > 0$. The noted $L_D(n)$ dependence on V_{GS} means that *L_{eff} is bias-dependent*. For strong inversion, n is high and L_D is relatively short, suggesting that

$$L_{eff(strong)} \cong L_g \quad , \qquad (2)$$

which is also consistent with the MEDICI simulation results (Figs. 2 and 3). The $L_{eff}(V_{GS})$ dependence reflected by (1) and (2) intimates a possible novel performance advantage for FinFETs. The longer L_{eff} in (1) implies lower I_{off} and better controlled SCEs, as evidenced by the measured characteristics in Fig. 8 where $L_g = 10$nm is significantly less than $L_{eff(weak)}$,

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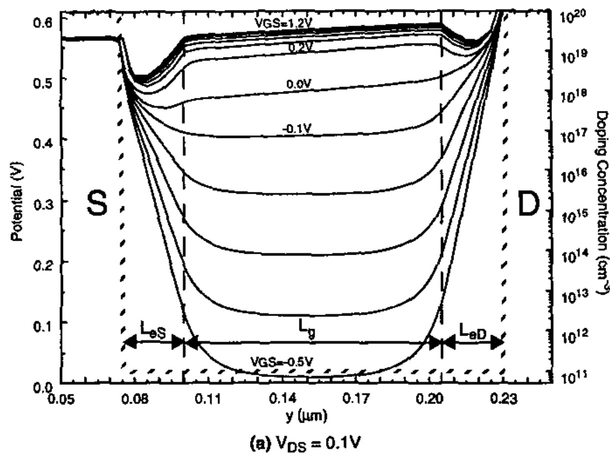


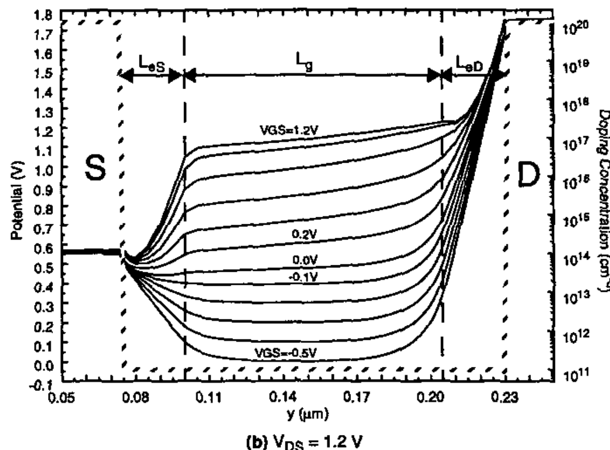
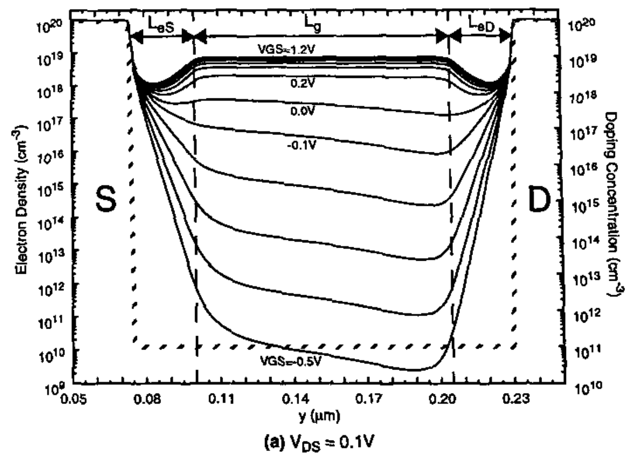


Fig. 2. MEDICI-predicted surface ($x = 0$, t_{Si}) potential variation between the S and D contact regions of an $L_g = 105$nm DG nFinFET ($V_t \sim 0$) for V_{GS} varying between weak and strong inversion, and for (a) low and (b) high V_{DS}; $t_{Si} = 26$nm. The entire S/D fin-extension regions ($L_{eS} = L_{eD} = 25$nm) were left undoped, as was the body/channel. The S/D doping profile is abrupt as shown by the dotted curve.



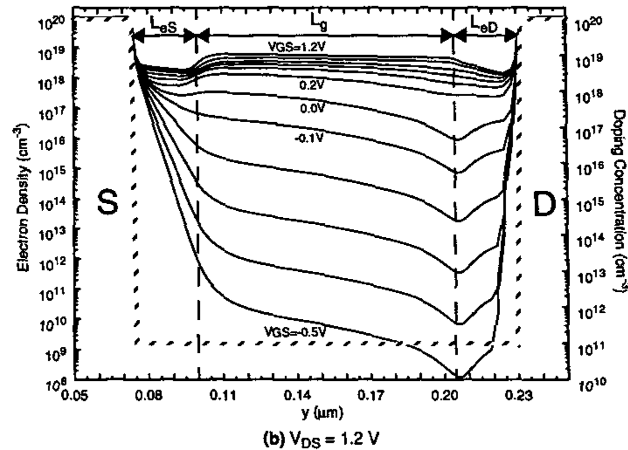


Fig. 3. MEDICI-predicted electron density (at $x = 0$, t_{Si}) variation corresponding to the potential variation in the $L_g = 105$nm DG nFinFET of Fig. 2.

while the shorter L_{eff} in (2) could mean higher I_{on} and lower gate capacitance, without parasitic components from the extensions, and no GIDL.

We note that the UFDG calibrations (Figs. 5 and 7) show the correlation between DIBL and S with $L_{eff(weak)}$ in (1). However, the UFDG calibrations to the measured data in strong inversion, with (2) enforced (Figs. 6 and 7), yield large, *effective* S/D resistances that are asymmetric and V_{DS}-dependent, posing a potential problem. In accord with the MEDICI-predicted $n(V_{GS}, V_{DS})$ in Fig. 3, these large resistances are actually indications of *non-ohmic* voltage drops (V_{eS} and V_{eD}) developed across both the L_{eS} and L_{eD} regions in support of I_{ch}, with V_{eS} being most critical because it reduces the effective gate voltage and thereby tends to restrict the inversion charge density and I_{on}. V_{eS} and V_{eD} are non-ohmic because the conductivities of the extension regions are bias-dependent and the carrier transport is *space-charge limited*, and, in fact, carrier velocity saturation in this transport can, as implied by the high electric fields ($E_e = -d\phi/dy$) in Fig. 2(b), define I_{on} if L_{eS} or L_{eD} is too long.

Hence, any exploitation of performance advantage implied by (1) and (2) will demand control of L_{eS} and L_{eD}, which, as defined by achievable S/D doping-density gradients in the thin-fin extensions and subject to avoiding punchthrough and/or random-doping issues, will not be easy. (Thicker-t_{Si} extensions would help.) Previous MEDICI-based studies [6] showed, in accord with the implied advantage, that nonzero L_{eS} and L_{eD} are optimal with regard to nanoscale DG CMOS speed, but no analysis of the underlying device physics was done. The dependences on L_{eS} and L_{eD} of the SCEs, I_{on}, and I_{off} are more complex than (1) and (2) imply. MEDICI-predicted SCEs shown in Fig. 9 for varying L_{eS}, but with ($L_{eS} + L_{eD}$) fixed in accord with FinFET technology [4], indicate that $L_{eS} = L_{eD}$ is the optimal configuration for SCE control, and that the SCEs are most severe when L_{eS} or L_{eD} is zero. Note that since S depends only on device geometry, the constant S for nonzero L_{eS} and L_{eD} in Fig. 9 confirms (1) for

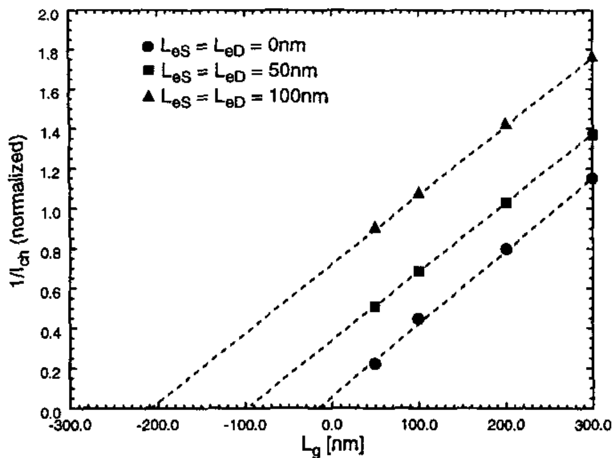


Fig. 4. MEDICI-predicted inverse weak-inversion channel current versus gate length of undoped DG nFinFETs with different S/D fin-extension (undoped) lengths; t_{Si} = 10nm. The L_g intercepts of the linear extrapolations indicate $L_{eff} = 0$ and confirm (1).

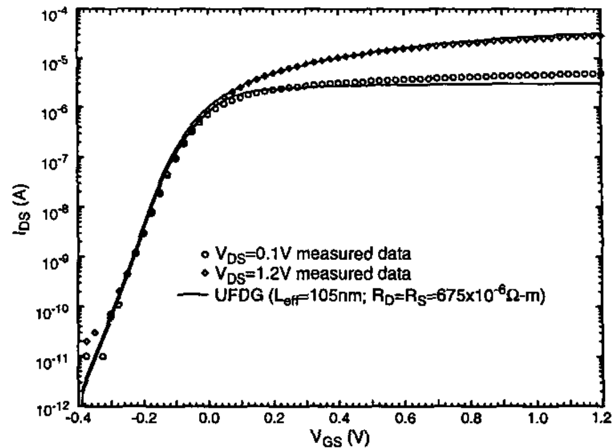


Fig. 6. Partial UFDG calibration to an L_g = 105nm nFinFET; t_{Si} = 26nm. With $L_{eff} = L_g$ (as in (2)) and very high, but constant S/D series resistance, the measured high-V_{DS} strong-inversion I_{DS}-V_{GS} characteristic is predicted well, but the low-V_{DS} and weak-inversion curves are not.

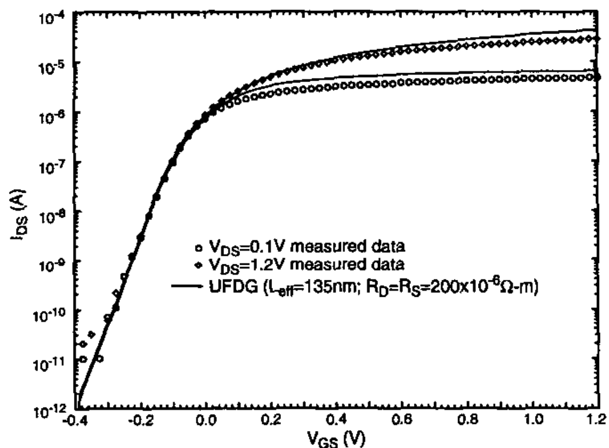


Fig. 5. Partial UFDG calibration to an L_g = 105nm nFinFET; t_{Si} = 26nm. With $L_{eff} = L_g$ + 30nm (as in (1)), the measured weak-inversion I_{DS}-V_{GS} characteristics are predicted well, but the strong-inversion curves are not.

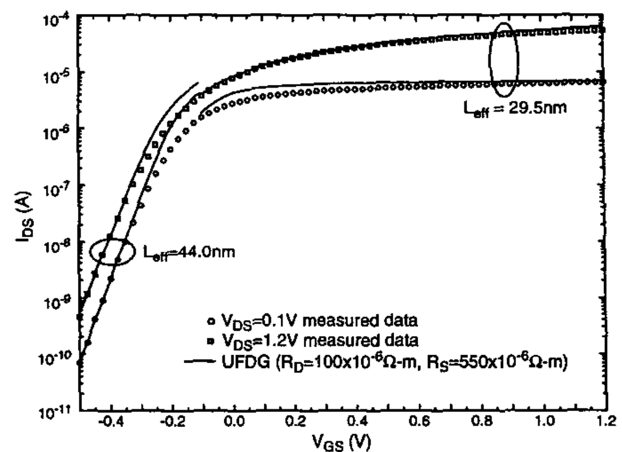


Fig. 7. Partial UFDG calibration to an L_g = 17.5nm nFinFET; t_{Si} = 17nm. With $L_{eff} = L_g$ + 26.5nm, the measured weak-inversion I_{DS}-V_{GS} characteristics are predicted well; with shorter $L_{eff} = L_g$ + 12.0nm (~$2L_D$), and very high source series resistance but low drain resistance, the strong-inversion curves are predicted reasonably well. However, *the bias-dependent L_{eff} and the non-ohmic V_{eS} and V_{eD} clearly must be modeled more physically.*

arbitrary gate position on the fin. However, note that DIBL and V_t depend on the gate position, the explanation of which involves $L_D(n)$ as well as the 2D effects. Although $L_{eS} = L_{eD}$ is optimal for SCE control, generally $L_{eS} \neq L_{eD}$ due to technology limitations [4]. Further, we find, based on our derived physical insights and MEDICI-predicted $I_{DS}(V_{GS}, V_{DS})$ characteristics accounting for the non-ohmic voltage drops, that $L_{eS} < L_{eD}$ (i.e., the gate positioned closer to the source) is optimal with regard to maximum I_{on}/I_{off}.

Compact Modeling

The insights revealed in the previous section imply novel compact modeling needed for nonclassical CMOS circuit design, as well as optimal FinFET design criteria. The bias dependence of L_{eff} is reflected by (1) and (2), but (1) must be refined (or tuned) based on the S/D lateral doping profile in the thin-fin extension, and on L_D there as indicated in Figs. 2 and 3. For strong inversion, L_{eff} in (2) will be a bit longer due to finite $L_D(n)$ near the channel, which suggests a secondary V_{GS} dependence that may be significant for extremely short L_g as implied in Fig. 7. Further, as implied in Fig. 9, L_{eff} for I_{ch} modeling could differ from that for SCEs.

Also, for strong inversion, V_{eS} and V_{eD} must be modeled. As can be inferred from Figs. 2(a), 3(a), 6, and 7, for low V_{DS} (and I_{DS}), the L_{eS} and L_{eD} regions can be modeled as constant resistances defined by carrier densities that have saturated with increased V_{GS} in accord with decreased $L_D(n)$ relative to

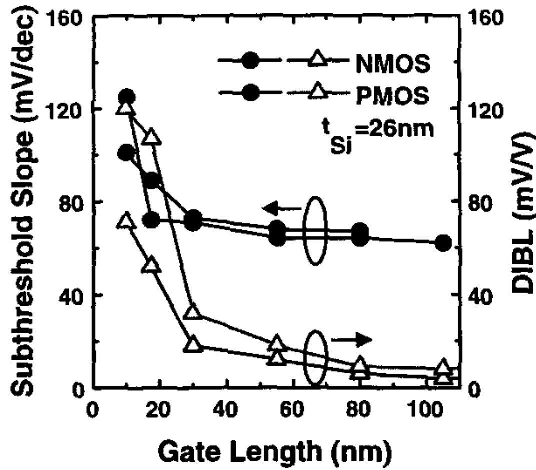


Fig. 8. Measured SCEs vs. L_g of CMOS FinFETs. The good control of DIBL and S in the nanoscale devices is due to $L_{eff} > L_g$, as approximated by (1).

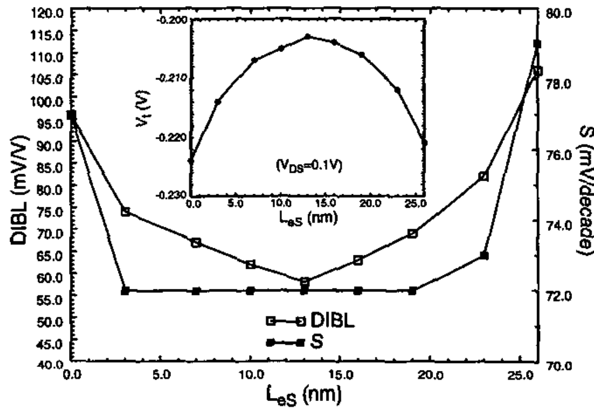


Fig. 9. MEDICI-predicted SCEs versus the source fin-extension length of L_g = 17.5nm DG nFinFETs for which (L_{eS} + L_{eD}) is fixed at 26nm; t_{Si} = 12nm. The entire S/D extensions and the body/channel were left undoped. The complex dependences on L_{eS} and L_{eD} are further reflected by the predicted linear-region threshold voltage (V_t) shown in the inset.

L_{eS} and L_{eD}, respectively. For high V_{DS}, Figs. 2(b) and 3(b) suggest that carrier-velocity saturation, with possible overshoot [9], in the L_{eS} and L_{eD} regions could define the saturation-region I_{ch}. To check this suggestion, we roughly calibrated MEDICI to the L_g = 17.5nm nMOSFET of Fig. 7, and monitored the electron velocity variation across the device. Indeed, as shown in Fig. 10, velocity saturation and overshoot are predicted in the fin-extension regions. So, for a fixed V_{GS}, which defines n in the regions as described above, the non-ohmic drops V_{eS} and V_{eD} will have to be modeled iteratively coupled to the channel-current analysis, similarly to the modeling of LDD voltage drops in high-voltage LDMOSTs [10]. The key expression for each region is

$$I_{ch} = -h_{Si}Q_n(V_{GS})v(E_e) \quad (3)$$

where Q_n is the integrated (over t_{Si}) inversion charge density

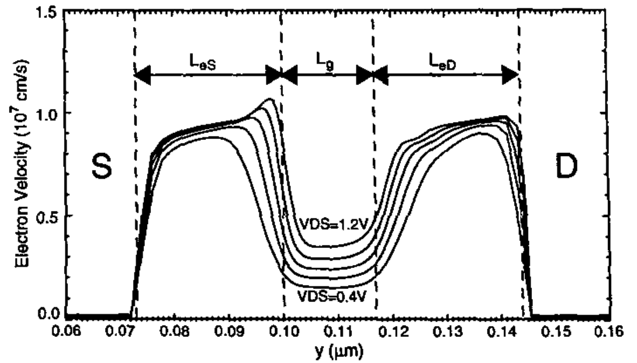


Fig. 10. MEDICI-predicted average electron velocity (at x = 0, t_{Si}) variation between the S and D contact regions of an L_g = 17.5nm DG nFinFET, comparable to that of Fig. 7, for increasing V_{DS}; t_{Si} = 17nm, t_{ox} = 1.7nm. The entire S/D fin-extension regions (L_{eS} = L_{eD} = 27nm) were left undoped, as was the body/channel. The S/D doping profile was assumed to be abrupt. With the energy-balance transport option on, MEDICI predicts velocity saturation, with some overshoot, in the fin-extension regions.

and v is the average carrier velocity, which saturates (at $v_{sat(eff)} > v_{sat}$ [9]) with increasing E_e. The integrals of E_e across L_{eS} and L_{eD} define the non-ohmic V_{eS} and V_{eD}, respectively, which iteratively [10] redefine I_{ch} in terms of (V_{DS} - V_{eS} - V_{eD}).

Summary

While alignment issues [4] regarding gate positioning may complicate the design optimization of nanoscale FinFETs as suggested here, the physical insights revealed (i.e., the unavoidable/needed gate underlap, the bias-dependent L_{eff}, and the non-ohmic fin-extension voltage drops) will aid pragmatic optimal FinFET design, as well as the development of a complete physics-based compact model that will be needed for optimal designs of nonclassical CMOS circuits.

Acknowledgments

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