Fast Switching Charge Dump assisted Class-D Audio Amplifier with high Fidelity and high Efficiency

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Abstract—A fast switching charge dump assisted Class-D audio amplifier is presented in this paper. To achieve high efficiency and high linearity, the Class-K* audio amplifier consists of the Class D amplifier with high efficiency and the proposed charge dump amplifier with high linearity. The charge pump amplifier works at faster switching frequency than Class D amplifier so as to compensate the distortion caused by switching of the Class-D amplifier. The Class-K* audio amplifier implemented in 0.35µm CMOS process shows -71.8 dB THD+N at 1 KHz and a maximum efficiency of 81% at an output power of 257mW for 4.1Ω load.

I. INTRODUCTION

Nowadays, portable electronic equipments such as PDAs, MP3 players, and DMB phones need a high fidelity audio power amplifier to drive a small loud speaker. This audio amplifier should have low power consumption, high efficiency and low distortion. To meet these requirements, the audio amplifiers can be realized with linear, switching or mixed-mode technique. The Class-AB is usually used as a typical linear amplifier. But this is not suitable for portable applications due to relatively low efficiency. To increase the efficiency, Class-D switching audio amplifier has been developed, but high frequency components caused by switching have to be filtered out at the output to accomplish good sound quality, increasing area and cost.

Thus, in this paper, we propose a new audio amplifier topology combining Fast Switching Charge Dump (FSCD) and Class D in order to achieve high efficiency and high fidelity. The proposed FSCD amplifier has better linearity and lower design complexity rather than Class-AB as a linear amplifier. It makes easily to implement in CMOS process. Moreover, a direct capacitor filter can be connected at the output side to absorb switching noise from Class D amplifier in the proposed topology.

II. PROPOSED FSCD ASSISTED CLASS D AUDIO AMPLIFIER

A. Architecture of FSCD assisted Class D Audio Amplifier

Fig. 2 shows a new hybrid audio amplifier employing FSCD technique to satisfy low distortion and high efficiency with simple design complexity. The proposed topology is similar to that of the Class K amplifier. But it is different because the proposed one is voltage-controlled voltage amplifier, while the Class K is current-controlled voltage amplifier. The proposed amplifier controls the error current to be zero, whereas the Class K controls the error voltage to be zero. Thus, we shall call this topology as Class-K* hereafter. Describing the features further, Class-K* is easier to implement than Class K since the sensing of the error voltage is much easier than that of the error current especially on high frequency switching environment. The high switching frequency components are directly filtered out by an output capacitor Cc. Also
excellent linearity is achieved with FSCD technique in this Class-K* rather than Class-AB as a linear amplifier.

B. Operation of FSCD assisted Class-D Audio Amplifier

The operation principles of the Class-K* amplifier are described as follows based on Fig. 2. In this topology, the sum of digital switching current (\(I_d\)) and compensation current of FSCD makes the output load current, and the output voltage is controlled by two control loops in parallel. The one is controlled by FSCD composed of \(g_m1\), COMP1, COMP2, MP2 and MN2 and forces the voltage of Ver1 to be zero. The other is controlled by Class-D composed of \(g_m2\), COMP3, MP1 and MN1 and flows most of the required output current to the load through MP1 or MN1. Unlike the MP1 and MN1, the switches MP2 and MN2 work independently. That is, as soon as the input signal rises over zero, MN2 turns off and MP2 does switching on and off according to the COMP1 comparing Ver1 with triangular wave, and dumps the charge into the output capacitor in parallel to the load. On the other hand, if the input signal falls under zero, MP2 turns off and MN2 does switching on and off according to COMP2, and power switch MN2 extracts charge from the output capacitor. Therefore shoot-through current induced by MP2 and MN2 cannot happen in this case. By operating MP2 and MN2 at high switching frequency, the ripple voltage at the output can be reduced to a small value. Also we can obtain the output voltage with low distortion by designing the bandwidth of the FSCD loop wide enough.

The direct charge dump operation of FSCD amplifier to compensate distortion dissipates some energy like a linear amplifier. However, this loss is slight in this case because most of the energy is supplied by the Class-D. We used FSCD amplifier rather than Class-AB as a linear amplifier because it has better linearity and lower design complexity. Moreover, a direct capacitor filter can be connected at the output side to absorb switching noise from Class-D.

C. Loop Analysis

As mentioned above, we can obtain the output voltage with low distortion by designing the bandwidth of the FSCD loop wide enough. In this topology, the output voltage is controlled by two control loops, \(T_1(s)\) and \(T_2(s)\), in parallel. Fig. 3 (a) shows the simplified block diagram of the proposed FSCD Class-D audio amplifier in order to analyze loop stability. In Fig. 3(a), the output load current \(I_o\) is the sum of digital switching current \(I_d\) and compensation current \(I_a\). That is, \(I_d\) supplies most of

\[
T_1(S) = \frac{\beta g_m1R_0}{V_m^1} \left( \frac{1 + s}{\omega_1} \right) \left( \frac{1}{1 + \frac{s}{\omega_1}} \right)
\]

\[
\omega_1 = \frac{1}{C_mR_m}, \quad \omega_2 = \frac{1}{C_1R_m}, \quad \omega_3 = \frac{1}{C_1R_f}
\]

, where \(gm1\) and \(R_m\) are the transconductance and the output impedance of error amplifier, respectively, \(1/V_m^1\) is the modulator gain in triangular wave generator 1 and 2, \(\beta\) is the feedback factor, \(R_{SW}\) is the impedance of FSCD power switches, \(C_m\) is the load capacitance, \(C_f\) is the output capacitance of error amplifier, and \(R_f\) is the compensation resistor.

In analysis of \(T_2(s)\), as loop of the FSCD \((T_1(s))\) has large bandwidth enough to compensate output distortion, it can be considered as ideal voltage source. Therefore, \(T_2(s)\) controlled by Class-D has transfer function as follows;

\[
T_2(S) = \frac{\beta g_m2R_0}{V_m^2} \left( \frac{1 + s}{\omega_1} \right) \left( \frac{1}{1 + \frac{s}{\omega_1}} \right)
\]

\[
\omega_1 = \frac{1}{C_mR_m}, \quad \omega_2 = \frac{R_0}{L}, \quad \omega_3 = \frac{1}{C_fR_f}
\]


, where $g_{m2}$ and $R_{o2}$ are the transconductance and the output impedance of error amplifier, respectively, $I/V_{g2}$ is the modulator gain in triangular wave generator 3, $L$ is the inductance, $C_p$ is the output capacitance of error amplifier, and $R_z$ is the compensation resistor.

Bode plot of $T_1(s)$ and $T_2(s)$ are shown in Fig. 3 (b) and (c), respectively. The dot line shows transfer function curve before compensation, and the real line is after compensation. As the real line curve, we have only to insert zero into close $\omega_p$ so as to guarantee loop stability because the proposed topology shows the two poles system in frequency response characteristic.

III. CIRCUITS AND IMPLEMENTATION

A. Op-amp and Error amplifier

In our design, the inverting amplifier A1 is added to make the input node of $g_{m1}$ virtual ground to reduce the design complexity and get high linearity in Fig. 2. To implement this amplifier, circuit shown in Fig. 4 is used in the proposed FSCD Class D audio amplifier [6]. The class AB biasing of the output transistors M1 and M2 is strongly controlled by two MOS translinear loops composed of M1, M3, M5, M6 and M2, M4, M7, M8, respectively. The class AB control circuit couples the gates of the output transistors in the quiescent mode of operation by generating low impedance. When M1 delivers a large current at load, M2 is regulated at a constant drain current and the gates of the output transistors are decoupling by generating large impedance. At the same time, however, the class AB biasing circuit steers the entire signal to the active output transistor. The class AB biasing circuit contributes to the noise and offset because no additional bias-current sources are required that would increase the noise and offset and also would reduce the gain.

To generate switching control signal for the FSCD and Class D, the error signal is integrated into capacitor $C_f2$ in error amplifier as shown in Fig. 2 or 3. The FSCD loop ($T_1(s)$) forces the voltage of $V_{err1}$ to be zero in Fig. 2. Then, input signal of $g_{m2}$ is nearly virtual ground. Also, the input node of $g_{m1}$ is virtual ground due to inverting amplifier A1. Therefore, as shown in Fig. 5, we use folded cascode operational amplifier with high gain and wide bandwidth compared with conventional 2-stage operational amplifiers. As this amplifier is absolutely one pole characteristic in frequency response, it is easy to design the bandwidth of the FSCD loop wide enough.

B. Band-gap Voltage Reference

The Band-gap Voltage Reference (BVR) schematic designed here is based on the conventional topology using $V_{BE}$ junction voltage in [3] and [4], as shown in Fig. 6 (a). In our circuit, the proportional-to-absolute-temperature (PTAT) current ($I_2$) in consideration of input-offset voltage is generated by $R_1$, $Q_1$ and $Q_2$, and is given by

$$V_b = V_a + V_{oss} = I_z R_z + V_z \ln \left( \frac{I_z}{N I_z} \right) + V_{oss} = V_z \ln \left( \frac{I_z}{I_{z1}} \right)$$  (3)

$$I_z = \frac{V_z}{R_z} \ln \left( \frac{N I_z}{I_z} \right) - \frac{V_{oss}}{R_z}$$  (4)

where $N$ is the size ratio of $Q_1$ and $Q_2$. The PTAT current which is mirrored by $M_1$–$M_6$ flows through $R_2$ and $Q_3$. Therefore, in node $V_{BGR}$, reference voltage insensitive to temperature becomes

$$V_{BGR} = \frac{K R_1}{2 R_z} \left[ V_z \ln (KN) - V_{oss} \right] + V_{BE3}$$  (5)

where $K$ is the current ratio of $Q_1$ and $Q_2$, $V_{BE3}$ is the junction voltage of $Q_3$.

We should consider the offset voltage produced by MOS transistor mismatch in the input stage of the amplifier. In a normal BVR circuit design, the effect of the amplifier input offset is reduced by a large $\Delta V_{BE}$. For offset robustness, in our design, $N$ and $K$ are 8 and 10, respectively. As a results, the voltage drop of $R_1(\Delta V_{BE})$
becomes 113mV. The OTA used to generate PTAT current is a 2-stage op-amp with high gain as shown in Fig. 6 (b). Simulated result for Temperature Coefficient (Tcf) in a range from -40°C to 125°C is 20 ppm/°C and shown in Fig. 6 (d). Fig. 6 (c) and (d) show generator circuit for ±400mV reference voltages and simulation results, respectively. In the simulation results, though reference voltage has ripple voltage at the moment of switching, it shows fast settling time for wanted reference value.

![Fig. 6. Folded cascade operational amplifier for error amplifier.](image)

The triangular wave generator is composed of three operational transconductance amplifiers (OTA), two resistors and one capacitor as shown in Fig. 7 (a) [6]. Both \( g_{m1} \) and \( g_{m2} \) connected in positive-feedback make a schmitt trigger. The saturation level is directly proportional to \( I_{B1}xR_1 \), whereas \( I_{B2}xR_2 \) define the threshold voltage of a schmitt trigger and time constant is proportional to \( I_{B3} \) charging the timing capacitor C. The waveforms associated with the generator are shown in Fig. 7 (b). From these waveforms, we obtain the oscillation frequency given by

\[
f = \frac{I_{B3}}{4CR_2I_{B2}}
\]

If MP2 and MN2 operate at high switching frequency, the ripple voltage at the output can be reduced to a small value. Therefore, in our design, switching frequency of MP2 and MN2 is chosen to be 10MHz and that of MP1 and MN1 to be 2MHz. The simulation results of both the triangular 1 and 2 operating in 10MHz with the dc offset of ±400mV, respectively, and the triangular 3 operating in 2MHz are shown in Fig. 8.

![Fig. 7. Circuit Diagram of the Triangular generator (a) and Output Waveforms (b).](image)

![Fig. 8. Simulation results of the Triangular generator.](image)

As mentioned in section II-B, the switches MP2 and MN2 work independently. Therefore shoot-through current induced by MP2 and MN2 cannot happen in this proposed audio amplifier. In Fig. 2, however, if the switches MP1 and MP2 operate according to COMP3...
without dead time, large shoot-through currents flow through the power transistors MP1 and MN1 from Vdd to Vss. This degrades power efficiency and damages the switches MP1 and MP2. Therefore, to decrease shoot-through currents induced in MP1 and MN1 at the moment of switching, we use gate driver with dead time as shown in Fig. 9 (a). Fig. 9 (b) shows waveforms of the gate driver with two dead time generators (td and td’, where td is the delay time for MP1 and MN1, td’ is the delay time for the previous drivers (MPPI, MNP1 or MPN1, MNN1) of the power switches). From these waveforms, MP1 and MN1 operate with non-overlap period.

The major advantage of the switching amplifier is excellent efficiency. There are three terms inducing power loss in switching amplifier. One is a conduction loss that is dissipated by on-resistance, another is a gate driving loss dissipated by charging and discharging the parasitic gate capacitance of the power transistor, and the other is switching loss that is dissipated in parasitic drain capacitance of the power transistor. Thus, total power loss equation is like as follows;

\[
P_{\text{total,loss}} = \frac{R_{\text{on}} I_{\text{O_rms}}^2}{N} + N (C_g + C_d) V_{\text{dd}}^2 f_{\text{sw}}
\]

(7)

, where \(R_{\text{on}}, C_g\) and \(C_d\) are the on-resistance, parasitic gate and drain capacitance per unit size (in our design, \(W/L = 10\mu\text{m}/0.35\mu\text{m}\)) of the power transistor, respectively, \(I_{\text{O_rms}}\) is the root-mean-square value of the maximum load current, \(N\) is the number of unit size, and \(f_{\text{sw}}\) is the switching frequency. The Eq. (7) is differentiated as to \(N\) to find minimum point of \(P_{\text{total,loss}}\), and then we obtain the optimum \(N\) of the power switch as follows;

\[
N = \sqrt{\frac{R_{\text{on}} I_{\text{O_rms}}^2}{(C_g + C_d) V_{\text{dd}}^2 f_{\text{sw}}}}
\]

(8)

Based on the Eq. (8), the physical size of the power switches MP1 and MN1 which occupy the most of the chip area are 70,000\(\mu\text{m}/0.35\mu\text{m}\) and 30,000\(\mu\text{m}/0.35\mu\text{m}\), respectively. On the other hand, the power switches MP2 and MN2 of the FSCD are determined by amount of compensation current for output voltage with low distortion, and in our design they are 1,200 \(\mu\text{m}/0.35\mu\text{m}\) and 320\(\mu\text{m}/0.35\mu\text{m}\), respectively. It is less than a fiftieth of MP1 and MN1. This shows that the proposed topology can be easily implemented occupying small area.

IV. MEASUREMENT RESULTS

The proposed Class-K* audio amplifier was fabricated with 0.35\(\mu\text{m}\) CMOS process, occupying a die area of 2 \(\times 1.46\) mm\(^2\) as shown in Fig. 10. The Class-K* amplifier operates with an inductor of 4.7\(\mu\text{H}\) having ESR of 100m\(\Omega\) and a capacitor of 100n\(\text{F}\) having ESR of 25m\(\Omega\) at dual supply voltage of ±1.65V. The measurement was done with the AP2722 audio analyzer at 4.1\(\Omega\) load, and the output is filtered out having the pass band from 10 Hz to 80 KHz.

![Fig. 11. Step response and Output voltage waveforms.](image)

Fig. 11 shows the step response for stability test (a), and the output voltage waveforms for sinusoidal input voltage of 100mVp (b) and 645mVp (c), respectively, at 1 KHz. These Figures show good stability and clean waveforms. The output voltage follows the input with the gain factor of 2.25.

![Fig. 12. THD+N versus input voltage](image)

Fig. 12 shows the THD+N versus sinusoidal input voltage for the frequencies from 20 Hz to 20 KHz. All of the plots have the similar shape and tendency of lower THD+N for higher output power. This is because the residual component of switching noise becomes negligible for higher output power. Especially at 1 KHz, Output spectrum with 114mW output power into 4.1\(\Omega\) load is shown in Fig. 13, and the THD+N is -71.8dB. The efficiency versus input voltage is shown in Fig. 14, and
the maximum power efficiency of 81% is obtained at an input voltage of 645mVp. The efficiency of the Class -K* audio amplifier is superior to that of the Class K [2] measured at a same condition.

![Fig. 13. Output spectrum with 114mW output power into 4.1Ω load.](image)

![Fig. 14. Efficiency versus input voltage.](image)

**TABLE I.** COMPARISONS BETWEEN CLASS-K* AND COMMERCIAL ICS.

<table>
<thead>
<tr>
<th></th>
<th>This Work (Class-K*)</th>
<th>Commercial Class D Audio amplifier ICs</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Supply Voltage (V)</strong></td>
<td>4.1</td>
<td>2.7 - 5.5</td>
</tr>
<tr>
<td><strong>Load (Ω)</strong></td>
<td>8</td>
<td>2.5 - 5.5</td>
</tr>
<tr>
<td><strong>Po (mW)</strong></td>
<td>257</td>
<td>2.7 - 5.5</td>
</tr>
<tr>
<td><strong>THD+N (%) at fin = 1kHz</strong></td>
<td>0.025</td>
<td>0.04</td>
</tr>
<tr>
<td></td>
<td>@ Vdd = 3.3V</td>
<td>@ Vdd = 3.3V</td>
</tr>
<tr>
<td></td>
<td>0.03</td>
<td>@ Vdd = 3.3V</td>
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<tr>
<td></td>
<td>0.04</td>
<td>@ Vdd = 3.3V</td>
</tr>
<tr>
<td><strong>Closed Loop Gain (dB)</strong></td>
<td>7</td>
<td>6</td>
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<tr>
<td><strong>Output Structure</strong></td>
<td>Half-Bridge-tied-load</td>
<td>Full-Bridge-tied-load</td>
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<tr>
<td><strong>Efficiency (%) at fin = 1kHz</strong></td>
<td>81</td>
<td>75 - 85</td>
</tr>
<tr>
<td></td>
<td>Class K</td>
<td>85</td>
</tr>
<tr>
<td></td>
<td>Class K*</td>
<td>80</td>
</tr>
<tr>
<td><strong>Switching Frequency (MHz)</strong></td>
<td>Class K = 2</td>
<td>25</td>
</tr>
<tr>
<td></td>
<td>FSCD = 10</td>
<td>1.45</td>
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V. CONCLUSIONS

We have proposed a fast switching charge dump assisted Class-D audio amplifier. The fast switching charge dump amplifier was introduced to reduce the distortion caused by Class-D amplifier, and it improved linearity of overall system. Based on the proposed topology, the Class D audio amplifier with -71.8 dB THD+N at 1 kHz and a maximum efficiency of 81% was demonstrated in 0.35µm CMOS process. The comparisons between this Class-K* amplifier and commercial Class D audio amplifier ICs are summarized in Table I. The Class-K* audio amplifier shows a superior sound quality with a similar performance in power efficiency.

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