P-42: A 10 bit Gray Scale Digital-to-Analog Converter with an Interpolating Buffer Amplifier for AMLCD Column Drivers

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Abstract

A 10 bit digital-to-analog converter (DAC) with an interpolating buffer amplifier is proposed for AMLCD column drivers. The proposed circuit is more effective than a conventional circuit in decreasing the DAC (Pass-Transistor Logic) area per channel. The average static current per channel is 1.8 \(\mu\)A and the average interpolating error rate in most of the gray range is a sufficiently small rate of 2.5 % (and less than 0.5 % in the mid-gray range). The uniformity of the channel output is also guaranteed by the proposed error-reduction technique.

1. Introduction

A TFT-LCD is the most popular flat panel display in various applications because of its thin shape, light weight, high resolution, and low voltage operation. With respect to large flat panel displays, in particular, the TFT-LCD has dominated the market for monitors and TVs that are smaller than 40 inches; moreover, this type of display has been steadily growing in panel size. However, besides wanting large screens and high resolution, customers want colors that are more natural. The color depth of display devices is determined by the number of colors that the device can represent, and the number of colors is related to the number of bits of a gray scale. Most medium or large LCD display devices have a 6 bit or 8 bit gray scale system to represent 256,000 or 16.8 million colors [1]. Nowadays, owing to customer demand for more natural colors, there is a need for a 10 bit gray scale system that can represent a billion colors.

To implement the 10 bit gray scale system, we need to develop a small DAC area. A typical 8 bit resistor-string DAC occupies more than 50 % of the whole column driver chip area, and a one bit increase in the gray scale doubles the area of the resistor-string DAC [1]. We therefore need to reduce the DAC area for a small column driver. To overcome this limitation, we propose a 10 bit gray scale DAC with an interpolating buffer amp. The proposed circuit not only reduces the DAC area, but also guarantees accurate channel output.

2. Prior Approaches to a 10 bit DAC in a Column Driver

The small area and accurate output of a DAC are the most important issues in the implementation of a 10 bit gray scale system. There were many ways to achieve these goals. Figure 1 shows various prior approaches to a 10 bit DAC in a column driver.

Figure 1(a) shows a conventional resistor-string DAC that uses a decoder and switches. In this circuit, a one bit increase in the gray scale doubles the size of the decoder (the number of switches) per channel. In addition, an 8 bit resistor-string DAC already occupies more than 50 % of the whole column driver chip area. Therefore, a 10 bit resistor-string DAC is more than four times larger than an 8 bit resistor-string DAC, and this difference in size leads to a rapid increase in the size of the whole chip.

To reduce the DAC area, the combination of an 8 bit resistor-string DAC and a 2 bit resistor-string DAC is proposed in Figure 1(b) [2]. In this circuit, the 8 bit resistor-string DAC generates two adjacent outputs and the 2 bit resistor-string DAC divides these two outputs into four levels. However, the use of an intermediate buffer amp to isolate each resistor-string DAC might become a problem because of its offset error. The offset error directly affects the channel output so that it is difficult to obtain a 10 bit DAC output that is both accurate and uniform.

To overcome the offset error problem in the intermediate buffer amp, the combination of the 8 bit resistor-string DAC and the 2 bit resistor-string DAC, which removes the intermediate buffer amp, is shown in Figure 1(c) [2]. In this circuit, although the offset error problem was solved, the loading effect of the second stage could affect the output of the first stage. To avoid this loading effect, the 2 bit resistor-string should be much larger than the 8 bit resistor-string; as a result, there was an additional increase in the DAC area.

Figure 1(d) shows how the input offset of the output buffer amp is used in the combination of the 8 bit resistor-string DAC and the 2 bit resistor-string DAC, which removes the intermediate buffer amp. Either VH or VL is applied to each positive input transistor according to the lower 2 bit signal. The difference between the input voltages of four positive input transistors divides the buffer amp output voltage into four levels so that the buffer amp operates as a 2 bit DAC. However, the output of the buffer amp suffers directly from the offset and mismatch error, making it difficult to obtain good output uniformity.

3. Proposed 10 bit DAC with an Interpolating Buffer Amp

Figure 2 shows the proposed 10 bit DAC with an interpolating buffer amp. This circuit requires an additional \(\Delta V\) reference, which means the difference between the output voltage of the 7 bit resistor-string DAC and its adjacent voltage. The VH reference means a 7 bit positive gamma reference and the VL reference means a 7 bit negative gamma reference. One \(\Delta V\) reference resistor-string can be applied to both the VH reference and the VL reference because the values of the VH and VL references are symmetrical with respect to the value of \(V_{com}\). This method therefore requires the VH reference, the VL reference and one \(\Delta V\) reference.

When the 10 bit data signal comes from the latch, the decoder selects the appropriate VH (VL) and \(\Delta V\) values for a higher 7 bit data signal. Because the VH (VL) reference and the \(\Delta V\) reference share the decoder logic, only one 7 bit decoder is required per channel, and the additional increase in the DAC area is just 2 switches for the \(\Delta V\) selection. In addition, the \(\Delta V\) values might be almost the same in certain ranges, such as in the mid-gray range.
of the VH (VL) reference. Thus, the number of the ∆V reference values can be reduced to less than half the number of VH (VL) reference values. Note that the addition of the ∆V reference is not as troublesome as expected.

In the second stage, the selected ∆V is converted to an appropriate current through the 3 bit current DAC. This current flows from (to) the resistor in the feedback loop of the buffer amp, and an appropriate voltage is added to (subtracted from) the VH (VL).

Figure 1. Prior approaches to a 10 bit DAC in a column driver. (a) a conventional 10 bit resistor-string DAC, (b) an 8 bit resistor-string DAC and a 2 bit resistor-string DAC with an intermediate buffer amp, (c) an 8 bit resistor-string DAC and a 2 bit resistor-string DAC without an intermediate buffer amp, (d) an 8 bit resistor-string DAC and a 2 bit DAC using an input offset of the output buffer amp.

Figure 2. The proposed 10 bit DAC

Figure 3. A block diagram of the system with the 7 bit resistor-string DAC and the 3 bit sub-DAC with an interpolating buffer amp.
The VH (VL) selected by the 7 bit pass-transistor logic is applied directly to the positive input transistor of the buffer amp. The ΔV selected by the 7 bit pass-transistor logic is converted to a current which is proportional to the ΔV through V-to-I converter. This current is divided through the 3 bit current DAC according to a lower 3 bit data signal. The divided current flows from (to) the channel output. In the case of the AH (AL) buffer amp, the 3 bit current DAC pulls (pushes) the current from (to) the resistor in the feedback loop of the buffer amp, and the voltage drops across the resistor R. The desired voltage for the data signal can be added to the VH (subtracted from VL) by controlling the current from the V-to-I converter and by controlling the resistor in the feedback loop of the buffer amp.

Figure 4 shows a conceptual schematic of the 3 bit sub-DAC with an interpolating buffer amp. The negative feedback loop is composed of the amp A1 and the transistor M1, and the voltage drop across the R1 has the same value as the ΔV, which is the positive input voltage of the amp A1. The current I, which is proportional to the ΔV, is generated through the R1, and the 3 bit current DAC divides this current into eight levels. In the case of the AH buffer amp, the divided current is directly pulled from the resistor R1. In the case of the AL buffer amp, the divided current is pushed to the resistor R2 through a wide-swing current mirror.

$$I_{\text{OUT}} = \frac{n}{2^N} \left( k \times \Delta V \right)$$  \hspace{1cm} (1)

$$V_{\text{channel}} = V_H + \frac{n}{2^N} \left( k \times \frac{R_2}{R_1} \right) \Delta V$$  \hspace{1cm} (2)

$$R_1 = k \times R_2$$  \hspace{1cm} (3)

Because the current I, which is generated by the kΔV reference and the resistor R1, has a minimum sub-μA value, the RC delay in the current DAC might become a problem. Furthermore, because ΔV should be added to VH (subtracted from VL) before the settling time of VH (VL), the RC delay in the current DAC should be minimized. In the proposed circuit, we designed the current DAC with the minimum cascode stack and optimized the size of the transistor and the bias voltage to reduce the RC delay.

To save the area and power consumption, we can remove the amp A1. In this case, the values of the ΔV reference can be calculated as follows:

$$\Delta V_{\text{REF}} = (k\Delta V) + \alpha$$

$$= (k\Delta V) + V_{\text{ref},M1} + \left( \frac{k \Delta V}{\frac{1}{2} \mu_n C_{\alpha} W \left( 1 + \lambda V_{DS} \right)} \right)$$  \hspace{1cm} (4)

Although the voltage drop across the R1 might vary due to process variations, these errors are also reduced by the 1/k factor in channel output stage.

### 4. Simulation Results

Table 1 summarized the simulation conditions and the performance of the 3 bit sub-DAC with an interpolating buffer amp. While assuming that the channel load has a resistance of 27 kΩ and a capacitance of 110 pF, we performed simulations with Cadence SPECTRE™. We also assumed a positive gamma range (7 V to 11 V), a negative gamma range (1 V to 5 V), and the value of Vcom to be 6 V. In Figure 4, the output buffer amp, AH (AL), was composed of a conventional two-stage op amp.

<table>
<thead>
<tr>
<th>Technology</th>
<th>0.35 μm CMOS (4M, 2P)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operating voltage</td>
<td>13.5 V(analog), 3.3 V(logic)</td>
</tr>
<tr>
<td>Load condition</td>
<td>27 kΩ / 110 pF</td>
</tr>
<tr>
<td>Static current</td>
<td>Min. 0.338 μA / channel</td>
</tr>
<tr>
<td>Max. 3.38 μA / channel</td>
<td></td>
</tr>
<tr>
<td>Interpolating error rate</td>
<td>Average 2.5%</td>
</tr>
<tr>
<td>Less than 0.5% in the mid-gray range</td>
<td></td>
</tr>
<tr>
<td>Color resolution</td>
<td>1 billion colors (10 bit)</td>
</tr>
</tbody>
</table>

Figure 5 shows the channel output with the 10 bit gray scale when the dot inversion was applied. We used the kΔV reference, which is k (=5) times the ΔV reference values. In the case of circle A, VH equals 9 V and ΔV equals 9 mV (the smallest value of ΔV). The 3 bit sub-DAC with the interpolating buffer amp divides 9 mV into eight levels. The results show that the channel output has an accurate 3 bit DAC output and the RC delay in the current DAC is small enough. In the case of circle B, VL equals 1.5 V and ΔV equals 90 mV. Moreover, 90 mV is accurately divided into eight levels.
Figure 5. Simulation results of the proposed 10 bit DAC

Figure 6. Comparison between the conventional 10 bit DAC and the proposed 10 bit DAC (a) the gray level–voltage curve, (b) an interpolating error (the difference between the conventional DAC and the proposed DAC)

5. Conclusion

To implement a 10 bit DAC in AMLCD column drivers, we first need to resolve some important issues. A conventional resistor-string type DAC cannot provide proper solutions for the DAC area and prior approaches to a small-sized 10 bit DAC have weak points such as a lack of output uniformity. The proposed 10 bit gray scale DAC, which consists of a 7 bit resistor-string DAC and a 3 bit sub-DAC with an interpolating buffer amp overcomes these limitations. The proposed 10 bit DAC circuit occupies a smaller area than the conventional method, and has immunity against the offset and process mismatch errors as a result of the proposed error-reduction technique. In addition, the higher bit sub-DAC (more than 3 bit) can be used in the mid-gray range because of its low interpolating error and accurate channel output.

6. References