P-43: A Multi-Chip Reference Current Generating Circuit for Current-Mode Column Driver ICs

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Abstract
A reference current generating circuit is proposed for current-mode displays using plural column driver ICs. The circuit supplies the uniform current with the column drivers. The cascaded circuits use an input reference current, sense it, and independently generate output currents in accordance with the current. The variation of generated output current in the reference current generating circuit of each column driver IC is reduced as compared with the conventional method. The generated output currents in column drivers have 0.1% error to the input reference current.

1. Introduction
A display driving system consists of column (source) drivers, row (gate) drivers, and a timing controller. A column driver IC of flat panel displays has several hundreds of channel outputs. In order to display medium and large-sized display panels such as those of monitors, notebooks, and TVs, the display system must include multiple column driver ICs. The column driver requires one or more reference circuits. In order to realize uniform display quality over the whole panel and reduce chip-to-chip variation, the accuracy of generated outputs in the reference circuits should satisfy the resolution of the display system. The accuracy of the reference circuit is important, because the difference between reference sources directly influences the quality of the display such as line and block dimming.

The output of the reference circuit serves as a reference voltage or current in the channel DAC of the column driver IC. The selected reference values are applied to pixel circuits, which represent images.

2. Prior multi-chip references
Depending on the display devices and driving methods, various multi-chip reference circuits are used [2-4].

3. Proposed current reference circuit
The proposed column driver ICs are arranged in cascade, as shown in Figure 2. A current source $I_{REF}$, which is an input current reference circuit, is supplied to the input port of the first column driver IC and flows from the input to output ports of all current reference circuits. Every reference circuit senses its input reference current and generates an identical output current. The reference circuits can independently generate output currents, because only one current source is used as an input reference current in each current reference circuit. The generated output current plays the role of the reference current in the column driver IC.

Figure 3 shows a conceptual diagram of the proposed reference current generating circuit. The gate, source, and drain voltage of

Current-driven displays, i.e., AMOLED displays, have many advantages when currents are programmed at pixel circuits. Variations of threshold voltage and mobility of thin film transistors (TFTs) are compensated during current programming to pixel circuits [1]. Meanwhile, a multi-chip current reference circuit is strongly required for uniform operation of current-mode medium and large-sized AMOLED displays. There are some existing methods to copy currents from one chip to another. Notably, production of a replica current by a current mirror [2] offers high accuracy between adjacent column driver ICs. However, the use of current mirrors repeatedly in a chain leads to problems in that the generated current includes accumulative errors arising from mismatched transistors. It is difficult to achieve generated currents with high accuracy among all column driver ICs. Another method is that, voltages across the reference resistor are applied across the internal resistor by using two amplifiers, the internal resistor and outputs of amplifiers generate output current [3]. However, the output current is affected by the offset voltages of the two amplifiers, and thus high voltage is required to reduce this effect. Meanwhile, in the case of the current sample-hold circuit [4], the gate-source voltage of a sample transistor, which includes the input current information in the current sample-period, is changed by the charge-injection in the current hold-period. Therefore, the output current is different from the input current and the value of the output varies in each chip due to charge-injection by chip-to-chip variation.

Figure 1. Voltage-mode column driver ICs arrangement for AMLCD

In the case of voltage-driven displays such as active matrix liquid crystal displays (AMLCDs), there is a resistor string in one column driver IC, as shown in Figure 1. Since voltage-taps of the resistor string are connected to each another in the column driver ICs, non-uniformity of reference voltages as a result of resistance mismatch is averaged out for all column driver ICs.

Figure 2. Current-mode column driver ICs arrangement

Figure 3 shows a conceptual diagram of the proposed reference current generating circuit. The gate, source, and drain voltage of
M1 are copied to those of M2. Assuming that M1 and M2 are matched, the current of M2 has the same magnitude of $I_{\text{REF}}$ flowing through M1.

Figure 3. Conceptual diagram of proposed reference current generating circuit

Figure 4 shows a schematic of the proposed reference current generating circuit. Through sensing the input reference current $I_{\text{REF}}$, the output current $I_{\text{OUT}}$ is generated. The circuit includes three negative feedback loops and a positive feedback loop. The negative feedback loop with A1-M1 and the positive feedback loop with A1-M2 are balanced by the negative feedback loop, because the negative loop gain is larger than the positive loop gain. Thus, the source voltage of M1 is copied to the source of M2 by A1. The source-gate voltage and size of M1 are equal to those of M2. If the effect of channel length modulation is negligible, the output current $I_{\text{OUT}}$ equals the input reference current $I_{\text{REF}}$. The current source $I_B$ and M3, which operates in the triode region, determine the source-drain voltage of M1 transistor by the negative feedback loop of A2-M3. This loop controls the drain voltage of M1 and the non-inverting input voltage of A1. If the magnitude of $I_B$ and $I_{\text{OUT}}$ are similar, M1 and M2 have similar drain voltages by the source-gate voltages of M4 and M5. The output current $I_{\text{OUT}}$ is transmitted to a current digital-analog converter through a current mirror of M6-M7, internally.

Figure 4. Proposed reference current generating circuit

(a) Current sink-type (b) Current source-type

Figure 5. Percentage error of difference between input reference current and generated output currents

Figure 5 depicts the simulation results for six current generating circuits in cascade connection assuming that six column driver ICs are used. The figure shows the difference between the input reference current and each generated output current from the six
current generating circuits. The generated output currents have a maximum error of 0.075% to the input reference current.

![Graph showing maximum current difference ratio vs. number of cascaded reference circuits](image)

**Figure 6.** Maximum percentage of error current according to the number of cascaded reference circuits.

Figure 6 shows the relationship between the ratio of the maximum error current and the number of cascaded reference current generating circuits. As the number of cascaded reference circuits is increased, the percentage error of difference between the input reference current and output current also increases. With 8 chips connected in cascade, 0.1% percentage error is achieved. The result satisfies the resolution specification for 10-bit operation.

Table 1 summarizes the achieved performance of the proposed reference current generating scheme and circuit. The circuit is implemented with a 0.35um CMOS process and 3.3V supply voltage.

<table>
<thead>
<tr>
<th>Simulation conditions and summary</th>
<th>0.35um CMOS (2P-4M)</th>
</tr>
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<tbody>
<tr>
<td>Technology</td>
<td>3.3V</td>
</tr>
<tr>
<td>Supply voltage</td>
<td>10µA</td>
</tr>
<tr>
<td>Reference current</td>
<td>90uA (+ I_{REF})</td>
</tr>
<tr>
<td>Static current</td>
<td></td>
</tr>
<tr>
<td>Maximum no. of cascaded column driver ICs</td>
<td>8</td>
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### 5. Conclusions

The applicability of the proposed reference current generating circuit is successfully verified with a Cadence Spectre simulation. By the operation of the negative feedback loops, independent operation of all reference current generating circuits in column drivers could be implemented. Chip-to-chip variation of the generated reference currents in column drivers satisfies 10-bit resolution operation. By using the proposed reference current generating circuit, the error of the generated currents in each column driver does not accumulate. The reference current generating circuit plays an important role in medium and large-sized AMOLED displays that use multiple column driver ICs.

### 6. References


