1. Introduction

In order to acquire a competence in competing with other flat panel displays which have already been dominating display market, a lot of efforts have been given to researches and developments for active matrix OLED (AMOLED) displays. Although AMOLED displays have discernable performance advantages such as a high contrast ratio, a fast response time, a very wide viewing angle, and thinness, there are some difficulties in implementing high resolutions because each pixel in a AMOLED display includes a plurality of transistors and one or more capacitors, in contrast, each pixel in a LCD has only one transistor and a few capacitors.

The resolutions of AMOLED displays, however, have been increasing rapidly and high pixel densities in AMOLED displays have been reported recently. State of the art works include displays with 188 ppi in a 4.3 inch VGA [1] and 223 ppi in a 1.8 inch QVGA [2]. In the latest report which reveals a display of 302 ppi, the AMOLED display utilizes laser induced thermal imaging (LITI) [3].

In recent years much interest has been focused on AMOLED displays as the ultimate display that will replace AMLCD applications. And of the several proposed driving schemes for AMOLED displays such as digital driving, voltage programming, and current programming, etc., current programming scheme reportedly minimizes the spatial variations of display pixel characteristics including threshold voltage and mobility dispersions in poly-Si TFTs [4].

For AMOLED drivers with a current programming scheme, very tight area constraint is imposed on the current DAC for each data driver channel in order to shrink the channel pitch for the current data driver in accordance with the increase in the display pixel density for AMOLED displays with high resolution as reported in the aforementioned literatures [1-3].

In this paper, an 8 bit cascaded-dividing DAC is proposed. It occupies less than one eleventh of the silicon area of a conventional binary-weighted DAC with the same resolution, and it operates at a low-voltage operation. The proposed DAC provides a good starting point in the optimization of the DAC area in terms of its performance and manufacturing die yield [5]. Furthermore, it simultaneously satisfies the requirements of a narrow channel pitch as well as high linearity and resolution for channel DACs.

2. Design and operation of the proposed DAC

If the current divider0 including a NMOS transistor pair (M1, M2) and a current source M0 shown in Figure 1 is considered, then it is clear that the current divider0 can divide the current Iref into two equal quantities Iout1 and Iout2 accurately, as long as the matching between M1 and M2 is sufficient and the two node voltages of the outputs Iout1 and Iout2 are identical.

In practice, however, the drain voltages of the current output nodes cannot remain identical and, when the voltages begin to diverge, the accuracy of the current division will be degraded. However, if M3 and M4 are added in the current divider 0 to make cascode connections with M1 and M2, respectively, the output current changes due to the voltage variations of the output nodes can be substantially reduced.

The output voltage coefficient (OVC) is a measure of maintaining the prescribed output current under varying output voltages [6]. By utilizing the OVC, the output current change of a cascode current divider is expressed as,
\[ OVC = \frac{\Delta I_{sat}}{I_{sat}} \sqrt{2 \beta_N \frac{V_{ds, sat}}{V'^2}} \]  

(1)

where \( \beta_N = \mu_N C_{ox} W/L \) and \( V_A = \lambda \) is the Early voltage. The typical values of NMOS transistor parameters \( V_A = 20 \) V and \( V_{ds, sat} = 100 \) mV, and the corresponding \( OVC = 1.25 \times 10^{-4} \approx 2^{-13} \). Hence, if for example there is a voltage difference of 1 V at the two output nodes, the accuracy of the current divider maintains a level of accuracy better than a 12 bit resolution. Therefore, if the cascade structure is used, there will be no accuracy problem up to 12 bits due to the output voltage differences in the current divider.

In contrast, a serious limitation comes from device mismatches. With modern CMOS technology, the current mismatching in a well-sized MOS transistor pair can be reduced to as low as nearly 0.3 \% and the current divider with cascode outputs can achieve an accuracy of up to 8 bit resolution.

To overcome the limitation from device mismatches and to obtain higher resolution for current DACs, a different current dividing scheme was proposed in which a switching-average technique was used to improve current dividing accuracy [7]. However, a high operating voltage of greater than 15 V was used in the design, adding to the complexity.

The schematic depicted in Figure 1 shows an area-efficient 8 bit cascaded-dividing DAC built with eight 1 bit current dividers in a cascade. As shown in the structure, the voltage allocation strategy of each cascaded current divider is very important for enabling the DAC to operate at a low supply voltage. If the resolution is extended to \( n \) bits, the \( V_{DD} \) voltage budget for an \( n \) bit cascaded-dividing DAC can be expressed as:

\[ V_{DD} = \sum_{i=0}^{n} V_{DS, Sat} + V_{DS, Sat \, Cascade} + V_{DS, Sat \, PMirror} + V_{th, P} \]

(2)

where all of the transistors for the current dividers are assumed to operate in the saturation region. For the first three terms in this equation, \( 2^{-i} (W/L)_i \) can be made constant by sustaining an identical current density. For the remaining terms, \( (W/L)_i \) are set to a constant value.

If \( n \) is sufficiently large, it is possible to neglect \( 2^{-(n-1)/2} \) in the parenthesis, and with the size ratios and parameters of the DAC design, which are \( (W/L)_3 = 2^2(W/L)_0 \), \( (W/L)_{PMirror} = 2(W/L)_0 \) and \( K_P = K_N/2 \), the \( V_{DD} \) expression is simplified as:

\[ V_{DD} = \sum_{i=0}^{n} V_{DS, Sat} + \frac{1}{\sqrt{K_N (W/L)_0}} \left( \frac{4 + \frac{1}{\sqrt{2}}}{1} \right) + V_{th, P} \]

(3)

With the design and model parameters of \( I_{ref} = 5 \mu A \), \( K_N = 1.19 \times 10^{-7} \, A/V^2 \), \( (W/L)_0 = 16 \), and \( V_{th, P} = 0.7 \) V, \( V_{DD} \) is obtained, and is nearly 1.16 V. Given a drain voltage margin of 100 mV for each MOSFET in the current dividers, \( V_{DD} = 1.16 + 0.1 \times 8 = 1.96 \) V for the 8-bit cascaded-dividing DAC. The suggested DAC structure is considered to be suitable for low-voltage operations.

### 3. Area comparisons and simulation results

Figure 2 shows the conceptual diagrams for comparing the chip area occupations of both the conventional binary-weighted DACs and the proposed cascaded-dividing DACs. In the area comparisons, only the areas occupied by the current sources are taken into count. For the digital control parts, both types of DACs have very simple digital control parts and require quite small chip areas, compared with typical thermometer-coded DACs. All the current sources comprising the DACs are assumed to be two-stacked cascoded ones.

![Figure 2. Conceptual diagrams of (a) a cascaded-dividing DAC, and (b) a conventional binary-weighted DAC](https://example.com/figure2.png)
resolution. It is obvious that the proposed cascaded-dividing DACs will occupy much less area than conventional binary-weighted DACs in implementing on chip.

Table I summarizes the comparison of the chip occupation areas. The cascaded-dividing DACs occupy very small areas in comparison with conventional binary-weighted DACs with equivalent resolutions.

An 8 bit cascaded-dividing DAC occupies less than one eleventh of the chip area of a conventional binary-weighted DAC with an equivalent resolution. Furthermore, the differences in the occupation area will increase rapidly as the resolution rise beyond 8 bits.

<table>
<thead>
<tr>
<th>Bits</th>
<th>Area occupations (unit area: $A_0$)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Conven. binary-weighted DAC</td>
</tr>
<tr>
<td>6</td>
<td>126</td>
</tr>
<tr>
<td>8</td>
<td>510</td>
</tr>
<tr>
<td>10</td>
<td>2046</td>
</tr>
<tr>
<td>12</td>
<td>8190</td>
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</table>

Table I. Area comparison of conventional binary-weighted and cascaded-dividing DACs

Table II summarizes the simulation results for the 8 bit cascaded-dividing DAC. The cascaded-dividing DAC achieves good DNL and INL performances of less than 0.15 LSB as shown in Figure 3. The simulation results show that the proposed DAC structure can operate normally on 2 V, utilizing 0.35 μm CMOS models for a 3.3 V-dedicated CMOS process.

The above simulations were carried out with Cadence SPECTRE simulator.

<table>
<thead>
<tr>
<th>Technology</th>
<th>0.35 μm (2P4M) CMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resolutions</td>
<td>8 bits</td>
</tr>
<tr>
<td>Power Supply</td>
<td>2 V</td>
</tr>
<tr>
<td>Power Dissipation</td>
<td>$12.4 \mu A \Delta I_{DAC,MAX} = 5 \mu A$</td>
</tr>
<tr>
<td>Sampling Frequency</td>
<td>1 MHz</td>
</tr>
<tr>
<td>DNL</td>
<td>0.13 LSB</td>
</tr>
<tr>
<td>INL</td>
<td>0.11 LSB</td>
</tr>
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Table II. Summary of simulation results of the 8 bit cascaded-dividing DAC

4. Conclusions

The proposed DAC is appropriate for current driving AMOLED drivers with demanding requirements such as a very fine channel pitch and high linearity and resolution performances for data channel DACs.

![Figure 3. Simulated INL and DNL in a 2 V operation with the utilization of 0.35 μm CMOS technology](image)

5. References


