High Power Factor Correction Circuit using Valley Charge-Pumping for Low Cost Electronic Ballasts

Gyun Chae, Yong-Sik Youn and Gyu-Hyeong Cho

Department of Electrical Engineering
Korea Advanced Institute of Science and Technology (KAIST)
Kusong-Dong, Yusong-Gu, Taejon, 305-701, Korea
TEL: +82-42-869-3424, FAX: +82-42-869-3410

Abstract -- A new cost-effective power factor correction(PFC) circuit, Improved Valley Fill (IVF) circuit combined with Charge Pumping Capacitors(CPCs), used in the electronic ballast for fluorescent lamps is proposed. The IVF can adjust the valley voltage higher than half of the peak line voltage. The CPCs draw the current from the input line to make up the current waveform during the valley interval. The measured PF and THD for a prototype electronic ballast are 0.996 and 5.5%, respectively.

1. Introduction

The fluorescent lamp is today's one of the most popular lighting system because of its higher luminous efficacy (lm/W) which is the energy conversion efficiency of the lamp. A ballast is needed for fluorescent lamps or gaseous discharge lamps because these have negative resistance characteristic in the desired region of operation [1,4]. Usually, in combination with capacitor, a lossless inductor or high-leakage transformer is used to compensate the characteristic of the fluorescent lamps. The electronic ballast plays the important roles of providing sufficiently high starting voltage, current limiting after starting, high input power factor, and reducing input line current harmonics.

Typical electronic ballasts have a bridge rectifier followed by an electrolytic energy storage capacitor to provide a nearly constant dc voltage to the subsequent high frequency resonant inverter driving the lamps. The resultant high frequency lamp current has low double line frequency modulation and has a current crest factor (CF) of about 1.5, which meets the traditionally acceptance limit of 1.7. However, this comes at the expenses of very low power factor (PF<0.6) and very high line current harmonic distortion (THD>130%) [1,5]. To obtain a unity power factor, low THD of the line current, and cost-effectiveness, a simple boost-type power factor corrector with a self-excited half-bridge type series resonant inverter is often used in the electronic ballast for fluorescent lamps [1,2,6]. However, the boost converter circuit increases the voltage stress to main device and is lossy and not cost-effective as they operate with high peak triangular shape current with additional power device, passive components and control circuit.

To solve the problems, a new improved valley fill (IVF) circuit combined with the valley boost converter(VBC) was proposed in [1]. The IVF circuit can control the valley voltage above half the peak line voltage by adjusting the value of reactor connected to the resonant inverter, preventing the pulsating line current around the peak and lowering double line frequency modulation of lamp current, i.e., lamp current crest factor(CCF). The VBC works during the valley interval only with simple controller, which decreases the losses of switching devices and the voltage stresses of resonant inverter[1]. However, in spite of the improvement of such a power factor corrector, there are some rooms for cost-effectiveness within the same power factor correction ability by reducing circuit elements.

In this paper, a new power factor corrector combined with the IVF in [1] and charge pumping capacitors connected to the resonant inverter is proposed to implement low-cost electronic ballast for fluorescent lamp. The measured PF and THD for a prototype electronic ballast are 0.996 and 5.5%, respectively, which are nearly the same results as those of the proposed scheme in [1].

2. Valley Fill (VF) and Improved Valley Fill (IVF)

Fig. 1 shows the basic diagram and waveforms of the input line current and DC bus voltage in the conventional valley fill circuit. The valley fill circuit is composed of two electrolytic capacitors(C1,C2), three diodes(D1~D3). Around the line peak, C1 and C2 are charged through D3 to the valley voltage which is half the peak line voltage. As long as the line voltage remains above valley voltage, the input line supplies the power to the ballast directly. When the line voltage falls below each capacitor voltage, i.e., valley voltage, bridge rectifier diodes are reverse-biased, and two electrolytic capacitors(C1, C2) supply the power to the ballast through D1 and D2. However, in this basic valley fill circuit, a pulsating

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line current happens to charge the capacitors near the peak line voltage, which deteriorates the PF(~0.95) and the THD(~40%). Also, the lamp current has high double line frequency modulation due to the large ripple dc bus voltage, which results in high current CF reducing the lighting efficiency and life of the lamps.

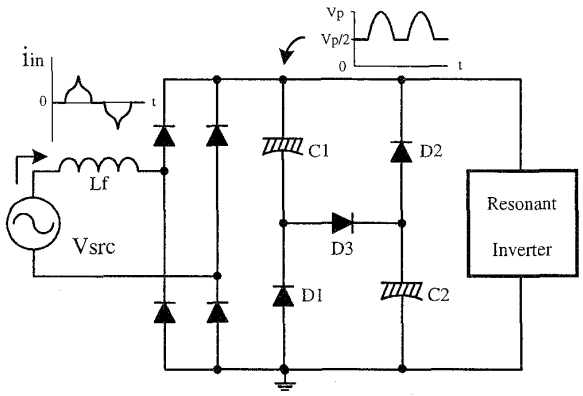

Fig. 1. Basic valley fill circuit

To eliminate the current spikes in the basic VFC, one more diode(D4) and a small capacitor(Cv) are additionally inserted to supply the charges to the electrolytic dc link capacitors(C1, C2) alternately according to the direction of the high frequency resonant inverter current as shown in Fig. 2, resulting in increased valley voltage higher than half the peak line voltage.

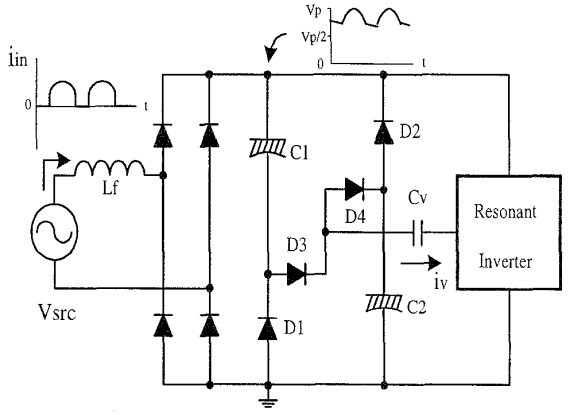

Fig. 2. Improved valley fill (IVF) circuit

As a result, the sum of the voltages across the dc link capacitors becomes higher than the peak line voltage, which prevents charging the dc link capacitors directly from line voltage around the peaks eliminating the current spikes in the line current waveform.

As long as the line voltage remains below C1 or C2 voltage (valley region), D1 and D2 conduct to supply the power to the resonant inverter. When the line voltage is above the voltage of C1 or C2 (direct region), the line supplies the power to the resonant inverter directly. During the direct region operation, C1 and C2 are charged alternately through a small capacitor (Cv) and one diode (D3 or D4) with the cyclic current generated by the resonant inverter. The capacitor Cv can be replaced by a small inductor whose reactance value controls the charging currents of dc link capacitors. If the reactance is high, the charging current of the dc link capacitors becomes small and the dc link capacitor voltages are nearly half the peak line voltage. On the other hand, if the reactance is getting lower, each capacitor voltage becomes higher above half the peak line voltage. Hence, the IVF can control each capacitor voltage (valley voltage) above half the peak line voltage by adjusting the reactance value, that is, the charging current of the dc link capacitors. The increased valley voltage helps to lower lamp flickering while the maximum DC-link voltage is limited to the peak of line voltage which is about 30% lower than the DC-link voltage of the conventional boost converter type PFC, reducing voltage stress to the main devices

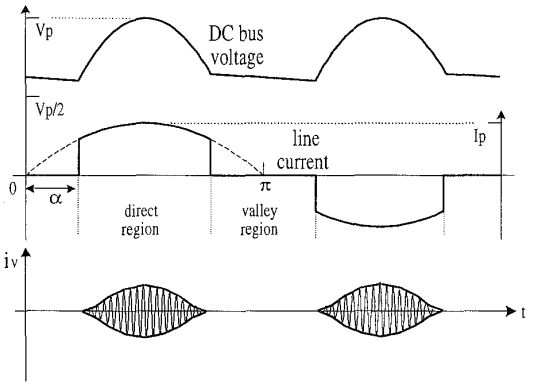

Fig.3 The operations of improved valley circuit with controllable nonconduction region

The dc bus voltage, the line current, and the charging current (iv) of the dc bus capacitors of Fig. 2 can be depicted as Fig. 3. The line current becomes a quasi sine waveform dependent on the nonconduction angle α. This is under the assumption that the ballast operates as a constant load, so the line current is directly proportional to the line voltage. This α is dependent on the amount of the charging current iv, and determines the valley voltage directly as

$$V_{DC\ bus,valley} = V_{line,peak} * \sin\alpha \ . \qquad (1)$$

The magnitude of the line current harmonics which represents only odd harmonic components, power factor(PF), and THD of the input line current are respectively given by

$$I_{n\ (1,3,5...\infty)} = \left(\frac{2}{\pi}\right)\left[\frac{\sin(n-1)\theta}{2(n-1)} - \frac{\sin(n+1)\theta}{2(n+1)}\right]_{\alpha}^{\pi-\alpha}$$

$$PF = \frac{I_{fund,rms}}{I_{total,rms}} = \frac{(\pi-2\alpha+\sin 2\alpha)/\sqrt{2}\pi}{\sqrt{(\pi-2\alpha+\sin 2\alpha)/2\pi}}$$

$$= \sqrt{\frac{\pi-2\alpha+\sin 2\alpha}{\pi}}$$

$$THD = \frac{\sqrt{\sum_{n=2}^{\infty} I_n^2}}{I_{fund}} = \frac{\sqrt{I_{total,rms}^2 - I_{fund,rms}^2}}{I_{fund,rms}}$$

$$= \frac{\sqrt{1-PF^2}}{PF} = \sqrt{\frac{2\alpha-\sin 2\alpha}{\pi-2\alpha+\sin 2\alpha}} \qquad (2)$$

Using eq. (1) and (2), PF and THD of the input voltage and current can be optimized. That is, the nonconduction interval α can be adjusted to set the valley voltage to be higher than half the peak line voltage by changing the capacitance value of Cv which controls the charging current (iv) of the dc bus capacitors. Even if the capacitor Cv is chosen to have the valley voltage nearly half the peak line voltage ($\alpha \approx 30°$ in eq. (1), (2)), the PF and the lamp current CF is more improved than that of the conventional valley fill of Fig. 1., which is resulted from eliminating the pulsating line current. The improved valley fill(IVF) circuit protects the direct current from the input line when the input line voltage is lower than the valley voltage.

Though the IVF improves the lamp current CF, the valley voltage has to be increased as high as posssible to minimize the lamp current CF for efficacy and lamp life. So a large α is required to increase the valley voltage. However, the PF decreases and THD increase as the valley voltage is increased. To solve the problem, a valley boost converter(VBC) combined with improved valley fill(IVF) circuit is suggested, which has good input line quality and lamp current characteristic as shown in Fig. 4 [1]. The limited operation of VBC during the valley region decreases the loss of switching devices and the size of power device and inductor and simplifies the control circuit. The measured PF , THD of line current, and lamp current CF was 0.997, 5%, and 1.5, respectively.

However, in spite of the improvement of such a power factor, there are soom rooms for cost-effectiveness within the same power factor correction ability by reducing circuit elements to meet custom requirements of low-cost products.

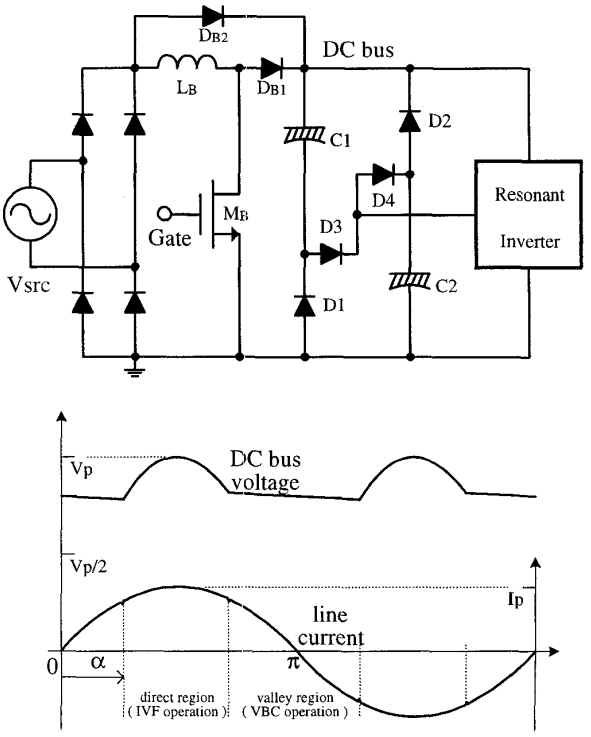

Fig. 4. Improved valley fill (IVF) combined with valley boost converter (VBC)

Therefore, we present a very simple power factor corrector combined the IVF with a pair of charge pumping capacitors which performs nearly the same power factor correction and reduction of line current THD.

3. The valley charge pumping (VCP) circuit

Fig.5 shows the electronic ballast with the proposed high power factor correction (PFC) circuit which is composed of a pair of charge pumping capacitors (Cp1, Cp2) and an improved valley fill DC-link. A pair of capacitors (Cp1, Cp2) are connected to the resonant inverter instead of using the VBC for PFC. The operations of the proposed VCP circuit can be explained in the two regions of the line voltage amplitude under the assumption that the charge pumping capacitors (Cp1, Cp2) do not affect to the operation of the resonant inverter.

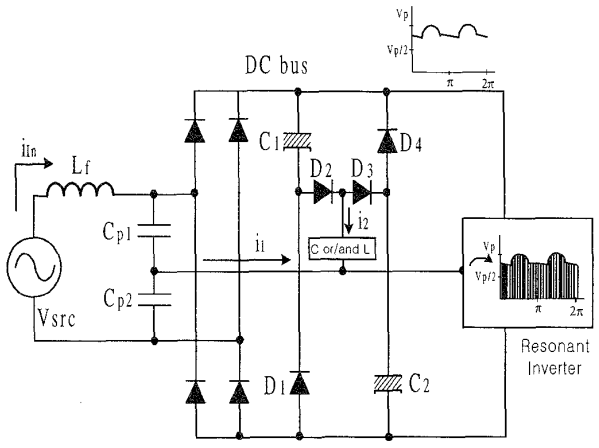

Fig.5 Proposed valley charge-pumping power factor corrector

During the period when the line voltage is higher than the valley voltage, the inverter current is almost directly supplied from the input line through the rectifier diode pairs, and the charging or discharging current (i1) of the charge pumping capacitors (Cp1, Cp2) does not affect to the line current waveform because the magnitude of each charge pumping capacitor current is lower than the direct line current. However, in the practical case, the current i1 is dependent upon the value of charge pumping capacitors and the line voltage magnitude. In case that the line voltage is lower than the valley voltage, the charge pumping capacitors (Cp1, Cp2) draw the line current from the input line as the voltage of the resonant inverter connected to the charge pumping capacitors changes with high frequency to make up the current waveform during the discontinuous valley interval of the valley fill circuit.

4. Operations of the VCP electronic ballast

The overall configuration of the electronic ballast with the proposed VCP circuit is shown in Fig. 6. The electronic ballast is composed of a typical self-excited half-bridge parallel loaded series resonant electronic ballast for one fluorescent lamp, IVF dc link and VCP circuit. The VCP and IVF are connected with the series resonant capacitor (Cr) of the resonant inverter. The operation of the entire ballast circuit can be explained in two regions of IVF operations which is similar to the mode analyses in [1]. Fig. 7 shows simulation results of the operation of the proposed electronic ballast during the region when the input ac source supplies the current to the resonant inverter directly. In this region, the dc bus capacitors C1 and C2 are charged alternately by the cyclic current (i2) generated by the resonant inverter. The input current is composed of the charge pumping current (i1) and the direct current through the rectifier diodes. The magnitude is dependent on the charge pumping capacitors (Cp1, Cp2).

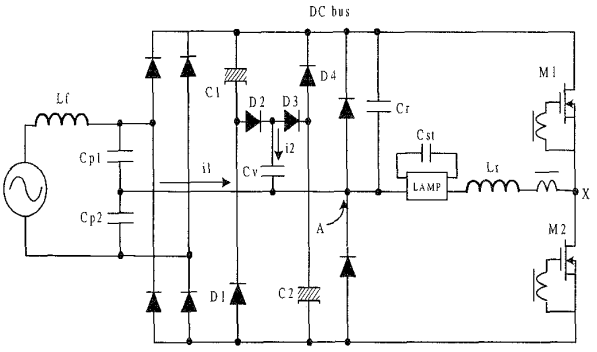

Fig.6 Overall configuration of electronic ballast for one fluorescent lamp

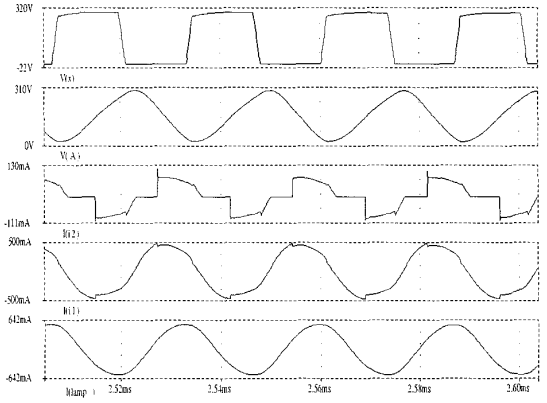

Fig 7 Simulation results of the proposed ballast during the direct region of the operation mode

Fig.8 shows the simulation results of the proposed ballast during the input ac source is nearly zero or below the valley voltage which is higher than that of the conventional valley fill. In this case, only the current i1 flows to make up the input line current. During the entire operation periods, the operation frequency of the ballast varies from about 25KHz to 33KHz according to the value of the dc link voltage in the two regions, which does not severely affect to the lamp characteristics. In [1], we verified that as the valley voltage is increased by controlling the nonconduction angle α, the PF of the input line current is decreased. Therefore, at the proposed PFC shown in Fig.6, the values of the capacitor Cv and VCP capacitors (Cp1, Cp2) must be selected carefully, especially Cv, considering the relationships between the PF and the lamp power and THD of line current. Fig.9 shows the

relationships among Cv, PF, and valley voltage of the circuit shown in Fig.6.

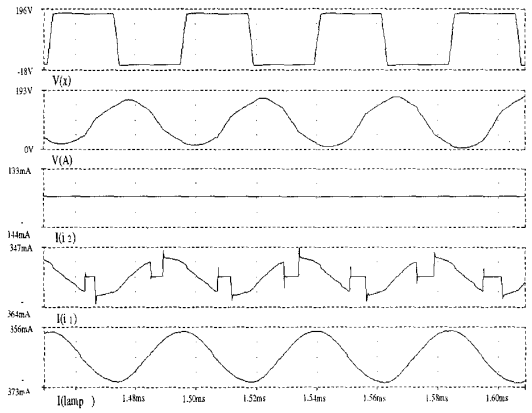

Fig 8 Simulation results of the proposed ballast during the valley region of the operation mode

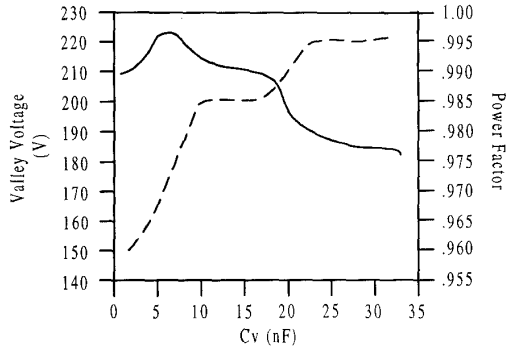

Fig.9 Relationship among PF, Cv, and valley voltage

5. Experimental Results

The proposed electronic ballast of Fig.6 is constructed and tested in the laboratory. The prototype ballast has been designed to operate at about 30kHz from an input line voltage of 220Vrms with an output for one 40W fluorescent lamp. The component values of the ballast under test are given in the following:

Lf=3mH, Lr=1.7mH
Cr=15nF, Cv=6.8nF, Cst=6.8nF
C1=C2=22uF, Cp1, Cp2=15nF
M1, M2 : IRF740 power MOSFET

Fig.10 shows the measured input line voltage and current waveforms. Fig.11 shows the oscillogram of the dc bus voltage and current i1 to verify the PFC operations during the periods of the line voltage. The input current has low harmonic distortion of 5.5% and measured input power factor of 0.996, which is successfully meet the IEC555-2 requirements. Fig.12 shows the waveforms of voltage of point A of Fig. 6, current i1 and i2 when the dc link voltage is near the peak of the line voltage to confirm the operations IVF capacitor (Cv) and charge pumping capacitors. Fig.13 shows the same waveforms of Fig.12 when the line voltage is lower than the valley voltage. In Fig. 13, the capacitor Cv does not operate to charge the dc link capacitors, but the charge pumping capacitors draw the line current to make up the waveform of the line current.

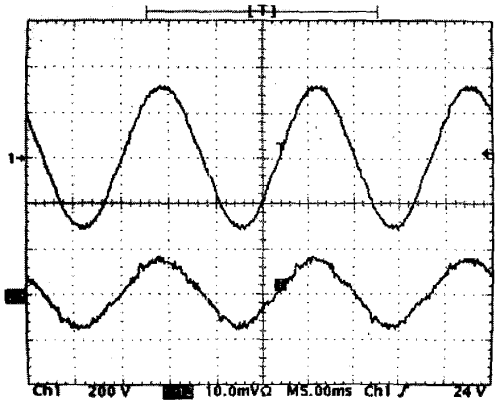

Fig.10 The input ac line voltage and current for the proposed ballast
(200V/div, 0.5A/div, 5ms/div, respectively)

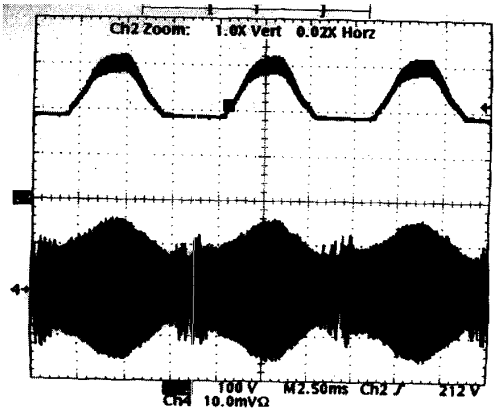

Fig.11 Experimental results of the dc bus voltage and current i1
(100V/div, 0.5A/div, 0.2A/div, respectively)

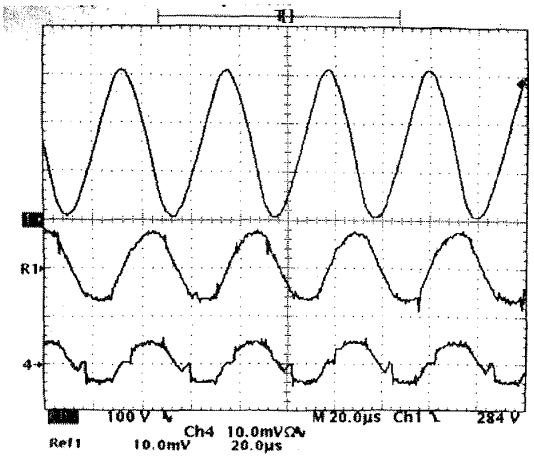

Fig.12 Experimental waveforms of the VA, i1, and i2 when the line voltage is nearly peak (100V/div, 0.5A/div, 0.2A/div, respectively)

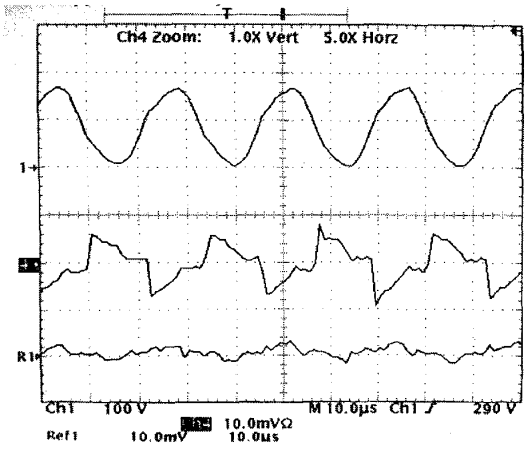

Fig.13 Experimental waveforms of the VA, i1, and i2 when the line voltage is below the valley voltage (100V/div, 0.5A/div, 0.2A/div, respectively)

6. Conclusions

A novel low cost, unity power factor electronic ballast is presented. The proposed ballast employs a pair of capacitors as charge-pumping elements combined with modified valley fill circuit having enhanced valley voltage instead of using the boost converter for shaping the input current, resulting in lower voltage stress on devices and higher efficiency. Experimental results prove that the prototype ballast successfully meets the IEC555-2 requirements for luminaries and suitable for low cost illumination systems.

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