High-frequency switching class-D power amplifier for portable sound applications

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Abstract— A 300mW single-chip CMOS class-D audio power amplifier employing new control methods is proposed. A high frequency modulator that is suitable for portable applications is adopted in this power amplifier. Zero voltage switching (ZVS) and adaptive power control (APC) are used to minimize the power loss. The new class-D amplifier chip is implemented using a standard 0.35µm CMOS process, and the test results are shown.

I. INTRODUCTION

Recently developed portable devices such as PDAs, MP3 players, and DMB phones employ a power amplifier to drive a small loudspeaker. The requirements for this power amplifier are low power consumption, high efficiency, and low distortion. The class-D audio amplifier has been developed to meet these requirements and has been improved significantly owing to advancing technology [1-3]. While the class-D amplifier satisfies the high efficiency requirement, it requires an output filter for good sound quality. Moreover, it has an EMI problem that is generated by a hard switching noise [4]. These problems adversely affect the applicability of the class-D amplifier to portable devices. In order to make this amplifier suitable for portable applications, the size of its output filter should be reduced. That is, the switching frequency of the class-D amplifier should be raised. However, the conventional class-D amplifier is limited in increasing the switching frequency, as it suffers from both a reverse recovery current loss and the aforementioned EMI problem. In order to overcome these problems, a Σ-Δ modulator power amplifier is proposed in this paper. Utilizing high-speed switching of the Σ-Δ modulator, the size of the output filter is reduced. The switching noise and power loss problems are solved via implementation of soft switching through a zero voltage switching (ZVS) power transfer circuit. In addition, the efficiency of the power amplifier is improved by utilizing an adaptive power control (APC) circuit. The proposed amplifier can operate up to 20MHz switching frequency. The maximum efficiency is 80% with a 4Ω speaker at 1% THD+N, and the lowest THD+N is 0.048%.

II. PROPOSED Σ-Δ MODULATOR CLASS-D POWER AMPLIFIER

The proposed class-D audio amplifier consists of a Σ-Δ modulator and a power transfer circuit, as shown in Fig. 1. The Σ-Δ modulator, which has a difference amplifier, an integrator and an over-sampling comparator, generates a quantized digital signal. From this signal, a unit power is delivered to the output load through the power transfer circuit.

There are several kinds of power transfer circuits. A switched-capacitor charge pump circuit is included, as shown in Fig. 2(a). However, this circuit is not suitable for this application, as its efficiency of the switched-capacitor circuit does not exceed 50%.

If an inductor is inserted in series with a capacitor C_o, the efficiency can be improved. However, it is difficult to control the switching timing due to the relationship between the switching and the resonant frequency. Hence, a current-controlled power transfer circuit, as shown in Fig. 2(c), is used for implementing the Σ-Δ modulator power amplifier. This circuit transfers power to the load in the form of a triangular current. This triangular current creates the ZVS, and this ZVS operation reduces the power loss.
resulting from high-speed switching. Additionally, it reduces the EMI problem.

\[ V_{ON}, V_{OFF} \] will transition in order to control MOS switches for ZVS operation. Using high-speed comparators and logic circuits, ZVS operation can be realized. This kind of ZVS switching does not generate any switching loss.

![Fig. 3 The operation of the current controlled ZVS](image)

### III. OVERALL CIRCUIT AND OPERATION

The overall circuit of the \( \Delta \Sigma \) modulator power amplifier is shown in Fig. 5. The triangular current is implemented by accurately sensing both the point where the inductor current becomes zero and the point where it reaches the threshold level (+Ith or -Ith). By doing this, the switching loss is minimized because the current through the parasitic capacitor \( C_p \) at node \( L_0 \) is charged and discharged through the inductor and recovered to the load. The reverse recovery current of the body diode of the MOS switch during hard switching is also eliminated by this ZVS switching. Thus, this kind of soft switching is essential in high frequency portable applications.

![Fig. 4 The timing diagram of the ZVS control](image)

![Fig. 5 Proposed \( \Delta \Sigma \) modulator ZVS power transfer audio amplifier](image)

Deciding the output switch size in the \( \Delta \Sigma \) modulator power amplifier is closely associated with the switching frequency. Although the switching loss is minimized by employing the ZVS technique, the gate driving power loss, which is expressed by \( C_i V_d^2 f \), increases due to the high
frequency switching of a maximum of 20MHz. Hence, the optimum switch size is determined by considering the sum of the conduction loss and the gate driving loss to be the minimum. In this high frequency operation, the optimum switch size was determined to be smaller than that with operation at lower frequency. Therefore, the turn-on resistance of the MOS switch was somewhat increased.

IV. PROPOSED APC OPERATION

In order that the output ($V_o$) follows the input ($V_{in}$) without any distortions, the average of the inductor current should be larger than that of the output load current ($i_o$). To be more precise, the threshold level of the inductor current ($i_{th}$) should be more than 2 times greater than the maximum of the output load current. However, if the amplitude of the load current is small, there exists a large conduction loss from the unnecessary power supply. In order to reduce this conduction loss, an APC circuit is proposed.

![Waveform of inductor current and conduction power loss](image1)

**Fig. 6** Waveforms of inductor current and conduction power loss

The APC circuit generates the threshold level of the inductor current from the error signal between the input and the output. Hence, the threshold level of the inductor current is adaptively varied by the input and output conditions. If the output signal cannot follow the input signal, the error will be larger and the APC circuit will cause the threshold level of the inductor current to increase. The unit power will then increase as well. On the other hand, if the error signal is small, the APC circuit will causes the threshold level of the inductor current to decrease. **Fig. 6** shows the inductor current waveforms and conduction power loss waveform with respect to the APC circuit. When the APC circuit is applied, the conduction power loss is greatly decreased.

V. VERIFICATION THROUGH EXPERIMENTAL RESULTS

**Fig. 7** shows the input, the output and inductor current waveform when the load is 4 Ω and the input is a 1 kHz sine wave source. The power supply used here is 3.3V. In order to minimize the external component size, a small- size inductor and a small chip capacitor are used. The inductance is 200nH and the capacitance is 1μF.

![Waveform of inductor current](image2)

**Fig. 8** Waveforms with rectangular input

![Waveform of inductor current](image3)

**Fig. 9** Inductor current waveforms with idle input
The responses of rectangular input are shown in Fig. 8 and inductor current with maximum frequency is displayed in Fig. 9 when input voltage is nearly zero.

Fig. 10 presents a graph of the THD. Each curve corresponds to a 100Hz, 1 kHz, and 10 kHz input source, respectively. When the output power is a quarter of its maximum output power, the THD is 0.048%. The maximum efficiency is about 80% in Fig. 11 and the maximum switching frequency is 20MHz in the experiment.

![Graph of Total Harmonic Distortion (THD)](image)

**Fig. 10** Total harmonic distortion (THD)

![Graph of Efficiency vs. Normalized Power](image)

**Fig. 11** Efficiency of the proposed amplifier

**VI. CONCLUSIONS**

A new class-D amplifier with a high-frequency modulator is proposed. The efficiency of the amplifier can be improved by ZVS and APC operation. This amplifier was implemented with a single chip using 0.35μm CMOS technology. The test results showed that the proposed audio amplifier could be made with exceedingly small size, a fast switching capability, and good sound quality compared with a conventional class-D controlled audio amplifier.

**REFERENCE**


