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Citation: Appl. Phys. Lett. 54, 2318 (1989); doi: 10.1063/1.101114
View online: http://dx.doi.org/10.1063/1.101114
View Table of Contents: http://apl.aip.org/resource/1/APPLAB/v54/i23
Published by the American Institute of Physics.

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Fabrication and characterization of lateral InP/InGaAsP heterojunctions and bipolar transistors

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(Received 13 February 1989; accepted for publication 29 March 1989)

We have investigated the fabrication of lateral InP/InGaAsP heterojunctions using both wet chemical and in situ melt-back etching and regrowth to form the device junctions. The current/voltage characteristics of the melt-back-etched and regrown heterojunctions exhibit ideality factors as low as 1.25. In addition, we have fabricated lateral heterojunction bipolar transistors with 2 \mu m base widths which exhibit a current gain of 6. These results indicate that regrown heterojunctions have adequate injection efficiency to form the active region of devices.

InP/InGaAs-based heterojunction bipolar transistors (HBTs) are attractive devices for both optoelectronic and high-speed digital circuit applications. In addition to their compatibility with long-wavelength optical components, the intrinsic transport properties of the materials comprising the transistor are superior to those of both GaAs and Si. However, one problem encountered with conventional HBTs is their mesa structure, which makes fabrication of low parasitic devices complex and surface planarization difficult to achieve. In particular, it is difficult to obtain a low extrinsic base resistance and a low collector capacitance using a vertical mesa approach. Minimization of both of these parameters is critical to the performance of high-speed circuits. In order to circumvent these problems, we have investigated an alternative technology for the fabrication of HBTs, in which we have introduced the idea of a lateral HBT formed using regrown base/emitter and base/collector junctions. In this letter we report on the electrical characteristics of InP/InGaAsP (InGaAsP energy band-gap wavelength \lambda_e = 1.3 \mu m) lateral (sidewall) heterojunctions prepared by two techniques: wet chemical etching and in situ melt-back etching to generate epitaxially grown (LPE) regrowth. We show that the melt-back-etched junction exhibits ideality factors comparable to those obtained with conventional junctions. An alternate fabrication technique for producing a lateral HBT, making use of impurity-induced disordering of a superlattice structure, has recently been reported. However, this approach requires a large impurity density to disorder the superlattice, which leads to high doping and the potential for impurity diffusion that would make it difficult to optimize HBT performance. In contrast, the approach described here, involving etching the base layer and regrowing the emitter and collector, is compatible with technologies used in semiconductor laser fabrication and we believe it represents a more flexible approach to the design of lateral HBTs.

A schematic diagram outlining the fabrication process of the lateral HBT is shown in Fig. 1. First, a 0.75- \mu m-thick, p = 5 \times 10^{16} \text{cm}^{-3}, InGaAsP (\lambda_e = 1.3 \mu m) layer was grown by organometallic chemical vapor deposition on a (100) oriented semi-insulating InP substrate. This layer will ultimately serve as the base layer of the transistor. Device isolation was achieved by wet chemically etching a region to define the contact area of the base and to roughly define the active base region. The wafer was then covered with 200 nm of SiO_2 and two areas, adjacent to the base layer, were opened to serve as both the mask for the intrinsic base mesa and the windows for the regrowth of the emitter and collector regions. After etching the sidewalls of the base mesa, by either wet chemical or in situ melt-back as discussed below, n-InP was selectively grown in the opened areas using LPE. The lateral HBTs fabricated by either technique had a base width of about 2 \mu m. Ohmic contacts were made to the n-type InP and p-type InGaAsP regions by alloying Au-Sn and Au-Be, respectively. A more detailed description of the fabrication process can be found in Ref. 4. A scanning electron micrograph of a lateral HBT, fabricated using melt-back etching and regrowth, is shown in Fig. 2.

Two techniques were investigated to etch the active region of the base mesa. The first made use of wet chemical etching using 3H_2SO_4:1H_2O:1H_2O, an etchant that selectively etches InGaAsP relative to InP. The second technique made use of melt-back etching inside the LPE reactor by placing the wafer in contact with an undersaturated Ga-In-As-P melt just prior to regrowth of the emitter and collector areas. It has been shown previously that melt-back etching of selected crystallographic planes can give optically flat surfaces. However, little or no information is available

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1) EPI-LAYER GROWTH

2) BASE MESA PATTERNING

3) IN - SITU MELTBACK ETCHING AND REGROWTH

4) LATERAL HBT

FIG. 1. Schematic diagram illustrating the critical processing steps used to fabricate a lateral heterojunction bipolar transistor.
The current/voltage characteristics of the lateral, wet chemical etched (dotted line), and in situ melt-back-etched (solid line) regrown heterojunctions are shown in Fig. 3. The transistor exhibits a maximum current gain of 6 at low current levels. While this is considerably below what is obtained for very narrow base width vertical transistors, this value compares favorably with results obtained for transistors prepared by wet chemical etching and regrowth, which typically exhibit current gains of 2. The dc current gain of the lateral HBTs is found to decrease slightly with increasing collector current density as a result of the high emitter resistance in this particular structure.

It should be noted that the minority-carrier diffusion length corresponding to a gain of 6 and a base width of 2 μm, is ~3.5 μm and this value compares well with what is obtained with bulk InGaAsP. In general, the base transport factor is limited by the electron lifetime in the base. Since in our prototype device a large area of the intrinsic base is exposed to the electrical properties of such an interface. The melt-back etching was achieved by contacting the substrate with an undersaturated In-Ga-As-P melt. Its composition was calculated using the formulas given by Kuphal: super-saturated by 5 °C, this melt would have yielded an InGaAsP layer lattice matched to InP with λv = 1.3 μm, i.e., of a composition similar to that of the base layer. A calibration run of the melt-back etch, using the same conditions as for the fabrication of the lateral HBT, yielded an etch depth of 200 nm after 10 s for an undersaturation of ~5 °C, with no undercut of the SiO2 mask observed.

The current/voltage characteristics of representative regrown heterojunctions prepared by the two etching techniques are shown in Fig. 3. The ideality factor of the melt-back-etched and regrown heterojunction is found to typically be 1.36 while that of the wet-etched and regrowth prepared junctions is typically 1.6. Some devices, prepared by melt-back etching, showed an ideality factor as low as 1.25. Indeed, although it is well known that perimeter recombination is much less in the InP/InGaAsP alloy system than, for example, in the GaAs/AlGaAs alloy system, the size of our active device area is only 0.75 μm × 8 μm, resulting in a perimeter to area ratio that is large enough so that perimeter recombination can have a considerable effect. With no effort made to passivate the exposed junction we believe our measured ideality factor represents an upper limit.

As expected from the current/voltage characteristics of the in situ melt-back-etched and regrown junction relative to the wet-etched case, the lateral HBTs prepared in this way showed higher current gain. Common-emitter characteristics (Ic vs Vce) of a lateral HBT having an emitter area of 0.75 μm × 8 μm and a base width of 2 μm are shown in Fig. 4. The transistor exhibits a maximum current gain of 6 at low current levels. While this is considerably below what is obtained for very narrow base width vertical transistors, this value compares favorably with results obtained for transistors prepared by wet chemical etching and regrowth, which typically exhibit current gains of 2. The dc current gain of the lateral HBTs is found to decrease slightly with increasing collector current density as a result of the high emitter resistance in this particular structure.

FIG. 4. Typical common-emitter characteristics of a lateral heterojunction bipolar transistor, prepared by in situ melt-back etching and regrowth. The transistor has a base width of 2 μm.

FIG. 3. Current/voltage characteristics of the lateral, wet chemical etched (dotted line), and in situ melt-back-etched (solid line) regrown heterojunctions.

FIG. 2. SEM micrograph of a lateral heterojunction bipolar transistor fabricated using in situ melt-back etching and regrowth.
the surface, we would expect substantial increases in the carrier lifetime by appropriately passivating the base region. In addition, significantly higher currents can be expected for devices with submicron base widths. While high current gains are important in some limited applications, gains in the range of 50–100 are more typical of what is required and obtained in high-frequency vertical mesa transistors.

Prior to this work, it had been widely believed that junctions prepared by etching and regrowth were not comparable in injection efficiency to conventional epitaxial junctions, i.e., had an ideality factor of the order of 2. In this work, we electrically characterized regrown lateral InP/InGaAsP heterojunctions prepared by wet chemical and in situ melt-back etching to establish that useful injection efficiencies, limited by surface recombination of the exposed junction areas, can be obtained. In situ melt-back etching was found to yield regrown junctions exhibiting typical ideality factors of 1.35, comparable to the value obtained for conventionally grown junctions with a similar perimeter-to-area ratio. A lateral HBT fabricated using this technique exhibited a current gain of 6. We believe that alternate realization of the device presently under investigation, in which the base is narrowed and the junctions are not exposed, will yield a significant performance enhancement.

The authors are grateful to G. K. Chang for useful discussions. Hoi-Jun Yoo is partially supported by the Korean Science and Engineering Foundation.