

# Top Electrode Vertical Cavity Front Surface Emitting Laser Diode (FSELD) for Optoelectronic Integrated Circuits Application

Hoi-Jun Yoo, J. R. Hayes, N. Andreadakis,  
E.G. Paek, G. K. Chang, J. P. Harbison and L. T. Florez  
Bellcore, RedBank, NJ 07701-7040  
and  
Young-Se Kwon  
Dept. of E.E., KAIST, Seoul, Korea.

Surface emitting laser diodes are of interest for optoelectronic integrated circuits because they can be fabricated using planar technology which does not require the wafer to be cleaved to form the laser mirror. Recently, there have been several reports of low threshold current operation using vertical cavity surface emitting laser diodes comprising a quantum well recombination region, high reflectance mirrors and tight current confinement to reduce the threshold current.[ref.1] GaAs/AlAs multilayers forming a  $\lambda/4$  mirror are widely used to form the high reflectance mirrors. However, they typically have a high series resistance and large step height which makes it difficult to integrate with other electronic and/or optoelectronic devices.

In this talk we will discuss a new SELD in which both the p-electrode and n-electrode, of the laser diode, are placed on the top surface and the total step height of the device is less than  $1\mu\text{m}$ ; as shown in Fig.1. It has a low series resistance and potential advantage of less absorption because the multilayer semiconductor mirror can be undoped. In addition, the laser light emits from the front surface leading to the possibility of having emission wavelength that are not restricted by the bandgap of the substrate. The fabrication process is compatible with that of HBT's[ref.2] and if a semi-insulating wafer is used as the substrate, device isolation can be easily obtained without deep groove etching.

The material that was used to form the top electrode FSELD was grown by MBE and comprised a stack of AlAs/GaAs bottom DBR mirrors doped n-type to  $5 \times 10^{18} \text{cm}^{-3}$ , an AlGaAs lower cavity layer, an InGaAs strained quantum well active region, an AlGaAs upper cavity layer and a p-type GaAs/AlAs top DBR mirror. This particular layer structure was fabricated into a "conventional" SELD by mesa etching the structure, for comparison with the top electrode FSELD that was fabricated using a process schedule described below after the top DBR mirror was removed. The top electrode FSELD was fabricated by performing a double ion implantation into the device epi-layer that was patterned with  $25\mu\text{m}$  diameter dots of a Si/Al<sub>2</sub>O<sub>3</sub> dielectric stack. The dielectric stack will initially function as the implant mask but will eventually act as the

stack. The dielectric stack will initially function as the implant mask but will eventually act as the top DBR mirror. An  $O^+$ -implantation was first performed to create a buried insulating layer. Following this, a heavy Be-implantation was undertaken to form a low resistance p-ohmic side contact to the active region. After exposition of n-DBR layers by wet chemical etching, Ni/Ge/Au/Ag/Au was deposited on the n-DBR layers to make an n-ohmic contact.

The top electrode FSEL D had a current/voltage characteristic that showed significantly less series resistance than a device fabricated from the same wafer having both top and bottom semiconductor mirror/contact stacks. In addition, the threshold current of the top electrode FSEL D was 6mA for a 25 $\mu$ m diameter device which compares favorably with the mesa etched SEL D that had a threshold current of 15mA.[Fig. 2] The top electrode FSEL D had an emission wavelength of 971nm and a spectral width above threshold of 5 $\text{\AA}$ . Only single mode operation was observed because the mode spacing is large in these short cavity lasers.

The top electrode FSEL D has a low operating voltage, small series resistance and low threshold current. In addition, since both the n-electrode and p-electrode are on the top surface of the wafer and the total step height is relatively low, this structure can be used in optoelectronic integrated circuits.

<sup>1</sup>J. L. Jewell, A. Scherer, S. L. McCall, Y. H. Lee, S. Walker, J. P. Harbison and L. T. Florez, *Electron. Lett.*, 25, 1123, (1989).

<sup>2</sup>P. M. Asbeck, D. L. Miller, R. J. Anderson and F. H. Eisen, *IEEE Electron. Dev. Lett.*, EDL-5, 310 (1984).

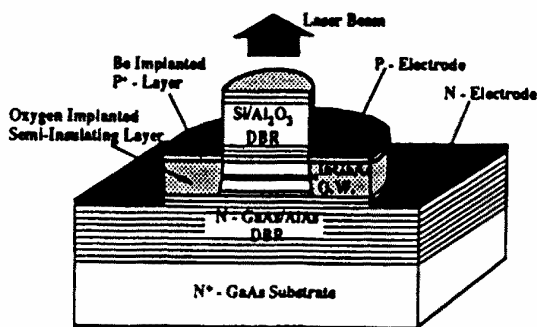


Fig.1 Schematic diagram of the top electrode FSEL D (Front Surface Emitting Laser Diode) fabricated by double ion implantation technique.

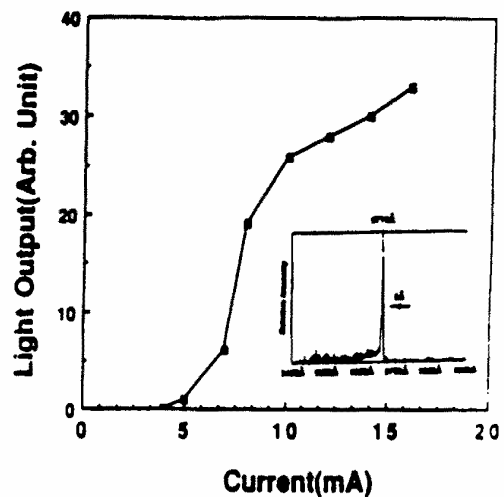


Fig.2 Light output and current characteristics and spectrum above threshold of the top electrode FSEL D under pulse mode operation.