Reduction of Direct-Tunneling Gate Leakage Current in Double-Gate and Ultra-Thin Body MOSFETs

Leland Chang, Kevin J. Yang, Yee-Chia Yeo, Yang-Kyu Choi, Tsu-Jae King, and Chenming Hu
Department of Electrical Engineering and Computer Sciences, University of California, Berkeley, CA 94720, USA
Phone: (510) 643-2638, Fax: (510) 643-2636, E-mail: leland@eecs.berkeley.edu

Abstract

The impact of energy quantization on gate tunneling current is studied for double-gate and ultra-thin body MOSFETs. The lower vertical electric field in the channel of these thin-body devices causes a reduction in gate leakage by as much as an order of magnitude. The additional effects of channel doping and high-κ dielectrics are also investigated.

Introduction

Continued scaling of transistor gate lengths may require the adoption of novel transistor structures [1] such as the double-gate (DG) or ultra-thin body (UTB) MOSFET [2] (Fig. 1). Such devices rely on the thickness of the silicon channel to control short-channel effects by eliminating any leakage paths far from the gate electrode. This may allow for scaling beyond the limitations of the standard bulk MOSFET design. Based on estimates of off-state drain leakage current, these advanced device structures could be scalable down to an ultimate limit of ~10 nm in gate length [3].

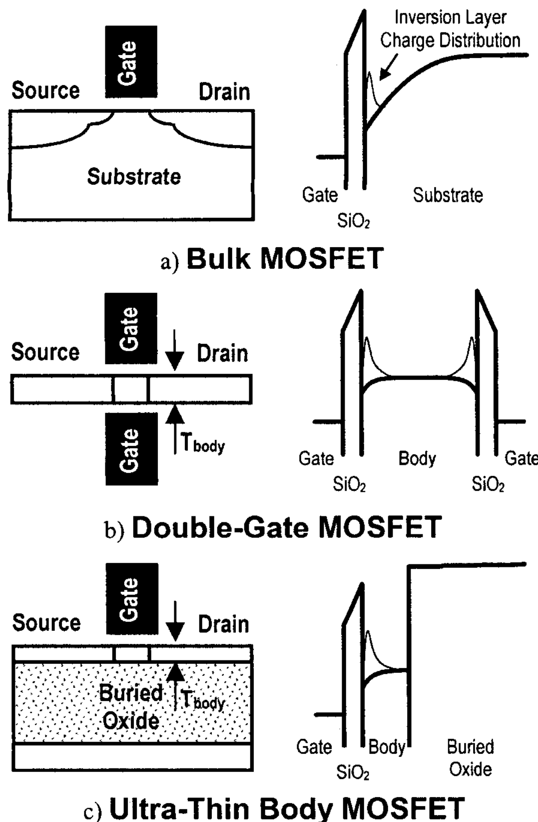

Figure 1: a) Bulk, b) Double-Gate (DG), and c) Ultra-Thin-Body (UTB) MOSFET structure cross-sections and energy band diagrams. A broader inversion charge distribution and reduced electric field away from the dielectric interface reduces gate leakage current.

In double-gate and ultra-thin body devices, control of short channel effects and threshold voltage is ideally achieved without the use of channel dopants. Depletion charge therefore cannot exist because there are no impurities in the channel. Since $Q_{depl}=0$ and $E_{eff} = (Q_{depl} + \eta Q_{inv})/\varepsilon_{Si}$ [4], carriers in the inversion layer thus encounter a smaller average vertical electric field than in standard bulk devices with heavy channel doping (Fig. 2). The field can be further lowered with thinning of the body (Fig. 3). A reduction in vertical field is expected to improve carrier mobility, especially as gate dielectric thicknesses are scaled and surface scattering mechanisms become dominant. Additional benefits may be apparent in gate tunneling current and device reliability.

In this work, the impact of reduced vertical field on gate tunneling current is studied. The effect of energy quantization due to carrier confinement in the thin body of these devices is first examined using a coupled Schrödinger-Poisson solver [5,6]. Reduction of the effective vertical electric field (E_{eff}) and lowering of the ground state energy (E_0) are first described. These effects are then applied to explain the reduction of direct-tunneling gate leakage current in thin-body SOI devices. The impact of body thickness, channel doping concentration, and dielectric material are investigated.

Impact of Energy Quantization

The behavior of the ground state energy at low and high gate bias is depicted in Figs. 3 and 4. Below threshold, band

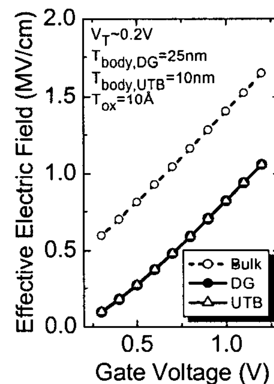

Figure 2: Vertical electric field (average of top and bottom of inversion layer) is reduced in DG and UTB devices.

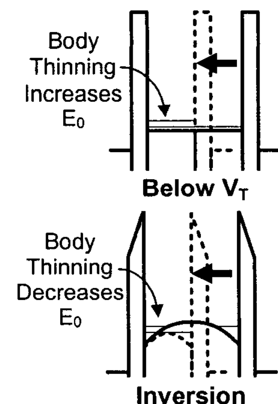

Figure 3: For DG and UTB, carriers are confined by a square well below V_T. In inversion, a triangular well forms.

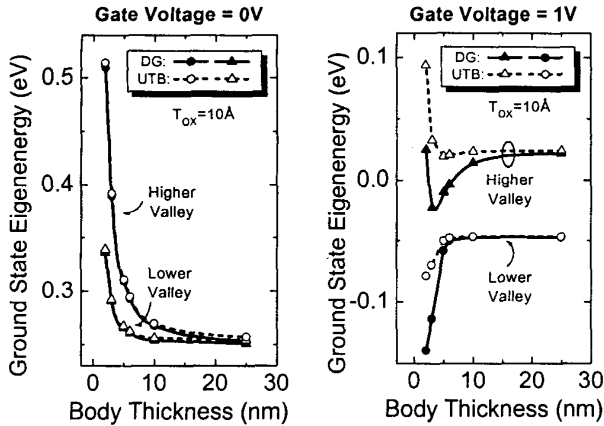

Figure 4: Below threshold, thinning T_{body} reduces the width of the square potential well, which further confines carriers and raises the eigenenergies. In inversion, the triangular well becomes shallower, thus pushing the energies downward. This effect is more significant in the DG case due to merging of the two inversion layers.

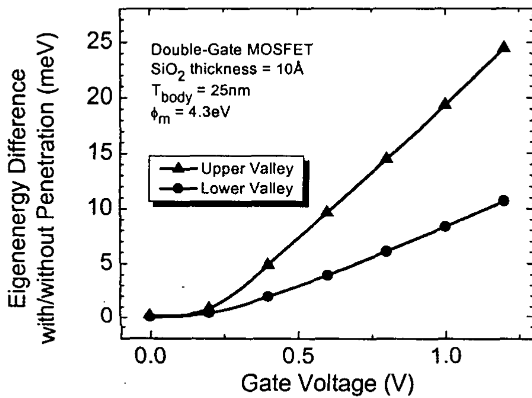

Figure 5: Electron wavefunction penetration into the gate dielectric is important as it reduces carrier confinement and lowers the eigenenergies. The difference in energy between cases with and without consideration of wavefunction penetration grows as gate bias is increased.

bending is negligible, and the structure can be approximated as a square well. As expected, the ground state energy increases as the body thickness is decreased, thus increasing the device threshold voltage [7]. In strong inversion, however, the inversion charge induces a semi-triangular potential well. As the body is initially thinned, the confining electric field and depth of the potential well are reduced (Fig. 3). As a result, the energies of eigenstates in the well are lowered. This effect is more pronounced in the double-gate case because merging of the two inversion layers further decreases the depth of the potential well. When the body thickness is very small (below ~3nm), the ground state of the higher valley is no longer bound in the triangular well and is instead confined by a square well. Thus, the higher valley ground

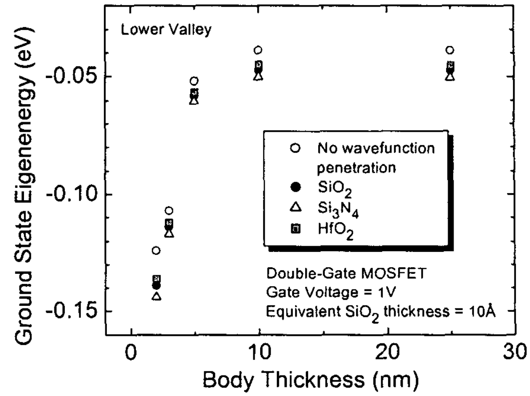

Figure 6: Inclusion of wavefunction penetration into the gate dielectric pushes the eigenenergies downward because of broadening of the wavefunction profile. Due to a difference in barrier height and effective mass, changing the dielectric material can change the magnitude of this effect.

state energy begins to increase with additional body thickness reduction, further splitting the lower and higher valleys.

Inclusion of electron wavefunction penetration into the gate dielectric lowers the eigenenergies because carriers are no longer perfectly contained inside the potential well. The eigenenergy difference obtained with and without consideration of wavefunction penetration can amount to as much as 10-20mV (Fig. 5). This difference increases with gate bias as the subband energies move closer to the conduction band edge in the dielectric, thus allowing for more of the wavefunction to penetrate into the insulator.

The amount of wavefunction penetration is influenced by the silicon-dielectric barrier height and carrier effective mass in the dielectric and can thus change with the choice of the gate dielectric material (Fig. 6).

Reduced Gate Tunneling Current

Previous experimental results have shown that gate leakage current in SOI devices is affected by the electric field distribution in the body [8]. Gate current was observed to decrease when a large positive voltage was applied to the substrate, essentially biasing the backside of the SOI in inversion and reducing the vertical electric field in the channel. Using potential profiles from a Schrödinger-Poisson solver [5,6], the transverse resonance method (TRM) [9,10] was used to investigate the physical mechanisms for this effect. By using a transmission line analogy, matching of the impedances seen by a carrier in the potential well yields complex values of carrier eigenenergies, $E_i = E_{ir} + i\Gamma_i$. The imaginary part of the eigenenergy is related to the lifetime of the quasi-bound state by:

$$\tau_i = \hbar / 2\Gamma_i$$

This can then be translated to gate tunneling current:

$$J_i = Q_i / \tau_i$$

where Q_i is the carrier population in the quasi-bound state. Summation of the current components over each carrier sub-

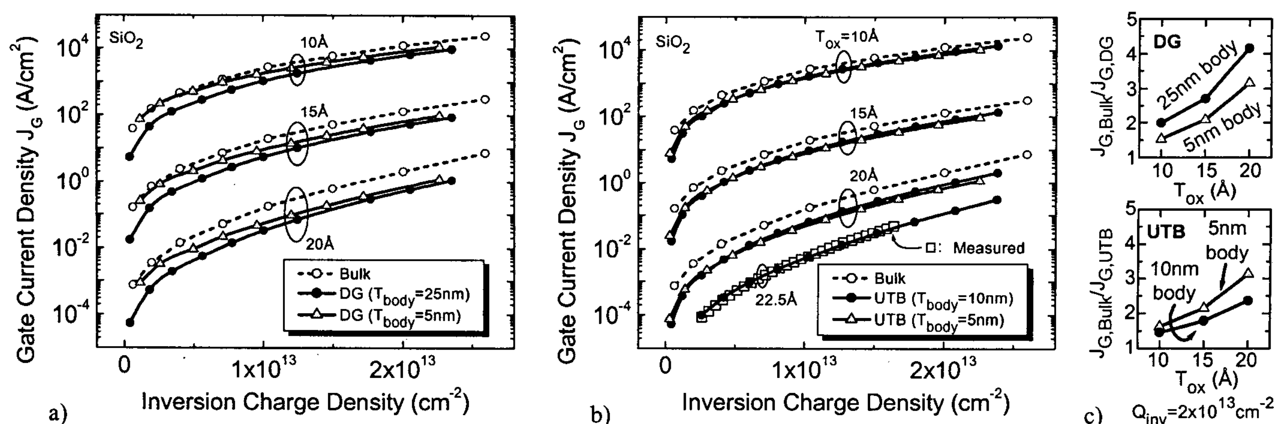

Figure 7: Comparison of gate current between bulk and a) double-gate, and b) ultra-thin body devices. Both DG and UTB MOSFETs show lower gate leakage due to reductions in vertical electric field and carrier confinement. Scaling of the body thickness enhances this effect. c) This improvement becomes less pronounced as the gate dielectric is thinned as the reduction factor drops considerably.

subband and valley yields the total gate current. Because this method considers the entire domain of the device structure, wavefunction penetration into the gate dielectric is allowed. However, the Schrödinger-Poisson solvers used to generate the potential profile do not consider this effect. Nevertheless, this inconsistency is expected to have only a minor impact on the potential distribution [11], thereby upholding the validity of this method.

In double-gate and ultra-thin body MOSFETs, gate current can be suppressed (Fig. 7) due to the reduced vertical electric field, which results in an increased lifetime of each quasi-bound state. In particular, the electric field near the bottom of the inversion layer is dramatically reduced, as can be seen in Fig. 1. Depending on device dimensions, gate current in a double-gate MOSFET can be reduced by up to 4x when compared with that of a bulk device. Gate current in an ultra-thin body MOSFET is reduced by up to 3x. At thinner physical dielectric thicknesses, this improvement is less pronounced because the quasi-bound state lifetime is more strongly affected by thin dielectric barrier than the shape of the potential well. As with the lowering of energy eigenstates, the reduction in gate current is enhanced in a double-gate device with decreasing body thickness due to merging of the two inversion layers.

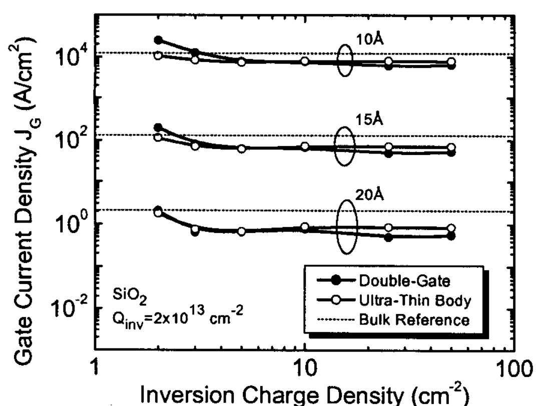

Figure 8: Dependence of gate current on body thickness for DG and UTB devices. Excessive thinning of the body (below a body thickness of ~5nm) increases confinement of carriers toward the gate oxide interface, and the gate current approaches that of bulk.

Scaling of the body thickness can decrease the gate leakage current because the potential well becomes shallower, as is seen in the UTB case (Fig. 7c). However, excessive scaling may increase the gate leakage current (Fig. 8) because the width of the potential well is reduced, thus confining the charge closer to the gate oxide interface and decreasing carrier lifetime. This effect is enhanced in the double-gate structure due to the symmetry of the problem. Below approximately 5nm in body thickness, gate current is seen to increase noticeably in both DG and UTB devices. This value is close to the practical limit of body thickness scaling [12], so this effect may not be of concern in actual device technologies.

Because threshold voltage control by adjustment of the gate work function remains a challenge, double-gate and ultra-thin body devices may need to depend on channel dopants to achieve appropriate values of the device threshold voltage [3]. Depending on the doping concentration, this can affect the electric field distribution in the body as a finite depletion layer can be formed when the channel doping is large. This, in turn, impacts the gate current (Fig. 9). With a p-type body (e.g. as needed for an NMOS device with an N^+ poly-silicon gate), a non-negligible depletion region forms beyond $\sim 10^{17}$ cm^{-3}, thus raising the electric field and increasing gate current. This threshold doping level is increased with a smaller body thickness because there is physically less space available to form a depletion region. An n-type body (as needed for an NMOS device with a mid-gap gate work function) can also alter the shape of the potential well and reduce the gate current when the doping concentration is extremely high.

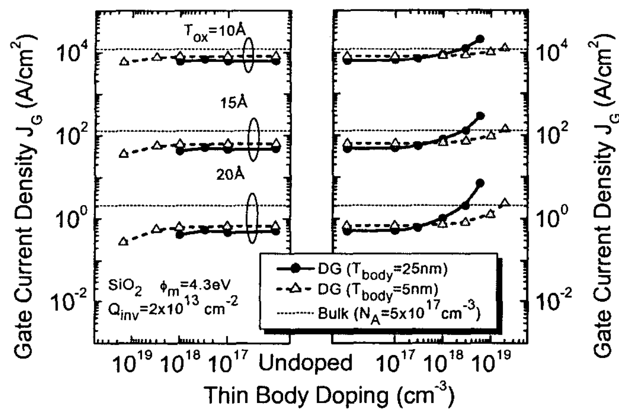

Figure 9: If channel doping is used to control V_T, the electric field in the body is altered. For an NMOSFET, a p-type body raises the electric field due to formation of a depletion region, thus increasing gate current. An n-type body can change the potential distribution and reduce the gate current at very high doping concentrations.

Gate Dielectric Scaling

In future technologies, high-κ materials may be used as the gate dielectric [1] to allow for increased physical thickness to reduce gate tunneling current. Gate leakage in the double-gate device structure with alternative gate dielectrics was investigated by the use of suitable values for the dielectric-silicon barrier height and effective mass in the dielectric [13] (Fig. 10). The increased physical thickness of the gate dielectric barrier makes the quasi-bound state lifetime more dependent upon the shape of the potential well. As a result, the reduction in gate current in the double-gate structure can exceed an order of magnitude at $T_{ox,eq}$=10Å with a dielectric such as HfO_2. It is thus predicted that the advantage of the DG and UTB structures is not only maintained, but also enhanced as device technology migrates to higher-κ materials.

A reduction in gate current means that the gate dielectric can be more aggressively scaled in double-gate and ultra-thin body devices at a given technology node than would be possible in a bulk design (Fig. 11). Assuming that Si_3N_4 will be the dielectric of choice for 25-70nm gate length technologies [13], switching to a double-gate MOSFET device structure can allow for up to an additional 0.8Å reduction in the effective oxide thickness.

Summary

Gate tunneling currents in bulk, double-gate, and ultra-thin body MOSFETs have been compared. Lower gate current for double-gate and ultra-thin body devices is attributed to reduced vertical electric field and quantum confinement effects. The gate dielectric can thus be more aggressively scaled in these advanced devices. The amount of improvement is affected by the body thickness and channel doping concentration. With the introduction of high-κ dielectrics, this reduction in gate leakage current will be enhanced.

Acknowledgements

This research is supported under MARCO contract 2001-MT-887.

References

[1] *International Technology Roadmap for Semiconductors*, 1999.
[2] H.-S. P. Wong, et al., *IEDM*, pp. 407-410, 1998.
[3] L. Chang et al., *IEDM*, pp. 719-722, 2000.
[4] A. G. Sabnis et al., *IEDM*, pp. 18-21, 1979.
[5] Schred 2.0, available at http://nanohub.purdue.edu/
[6] Available at http://www-device.eecs.berkeley.edu/qmcv.html
[7] Y. Omura et al., *EDL*, pp. 569-571, December 1993.
[8] L. T. Su et al., *IEDM*, pp. 349-352, 1992.
[9] A. N. Khondker et al., *J. Appl. Phys.*, pp. 327-337, 1998.
[10] S.-H. Lo et al., *EDL*, pp. 209-211, May 1997.
[11] H. Iwata, *Jap. J. Appl. Phys.*, pp. 4496-4500, July 2001.
[12] D. J. Frank et al., *IEDM*, pp. 553-556, 1992.
[13] Y. C. Yeo et al., *EDL*, pp. 540-542, 2000 and unpublished data.

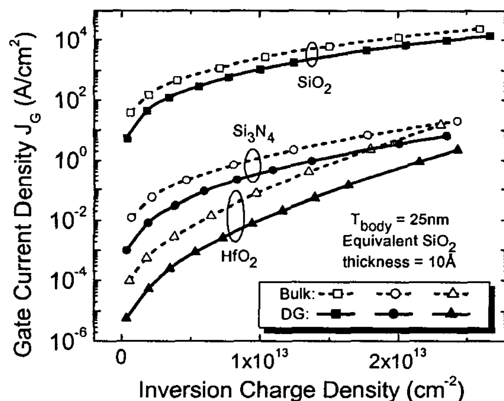

Figure 10: With the projected shift to alternative gate dielectrics, the gate current improvement from bulk to double-gate can be larger. The thicker physical thickness of the dielectric makes the carrier lifetime a stronger function of the electric field distribution, which is lower in DG and UTB.

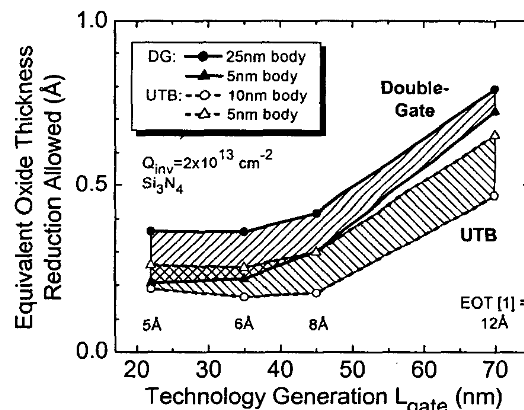

Figure 11: The reduction in gate current in DG and UTB devices means that the gate dielectric can be thinner than for a bulk MOSFET. Si_3N_4 is assumed as the dielectric material for 70nm gate-length technologies and below [13].