Effect of Power Distribution Network Design on RF circuit performance for 900MHz RFID Reader

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Abstract

In these days, radio frequency identification (RFID) has been widely believed that it brings a revolution in the main distribution industry substituting barcodes. Especially, as the demands for mobile RFID applications increase, there has been strong need for integrating RFID system keeping small size and low power dissipation. Thus, digital, RF, and analog chips have been integrated into one package under the name of system-in-package (SiP). However, there are various problems to integrate the RFID system into a package. One of those problems is undesired noise coupling from digital to analog circuitries through power distribution network (PDN). In this paper, we analyze the effect of power distribution network design on RF circuit performance by using both simulation result and measurement result.

1. Introduction

In RFID systems, power ground switching noise is mainly generated by digital circuit blocks, and it is significantly coupled to the analog and RF circuits on various paths, such as chip, package, and board level. Even though RF and analog blocks have been isolated from power ground of noisy digital blocks using power ground split, we could not perfectly remove noise coupling path, as seen in Fig 1 (a). The coupled digital switching noise affects power ground of analog and RF circuit blocks, as shown in Fig 1(b). And it directly degrades the overall system performance of the RF systems, such as noise figure, gain, and linearity. Therefore in order to guarantee the system performance, we should design PDN of RF and analog blocks carefully.

For the purpose of isolating RF and analog blocks from digital switching noise, several techniques such as split power ground plane, decoupling capacitors, and electromagnetic band gap (EBG) structure have been used.

In this paper, we have investigated the effect of PDN design on RF circuits, which have been designed for the front-end of a 900 MHz RFID reader. Moreover, design methodologies have been considered on the effect of the on-chip decoupling capacitors and off-chip decoupling capacitor. To verify the effect of decoupling capacitors on the RF performance, we have incorporated models of the chip, and test board into simulations simultaneously. And we have fabricated the chip and test board, and measured the RF output waveforms.

Fig 1. (a) Concept of capacitive noise coupling from noisy digital power ground to RF and analog power ground in board level (b) Concept of output waveform distortion of mixer due to coupled digital power ground noise

2. Models of PDN and RF Circuits

Figure 2 (a) shows a schematic of test board for modeling. Test board model consisted of 4 layers stack up, and it had power ground plane whose dimension is the size of 50mm by 77mm. Figure 2(b) describes CMOS chip model connected to the test board model. The size of the chip model was 2.5mm by 2.5mm. There are two kinds of chip models : RF circuit models and power ground network models. We modeled mixer and low noise amplifier (LNA) as shown in Fig 2(c-d). They designed as cascade type and mixer designed as double balanced type, respectively. The power ground network models included wide power ground wires, on-chip decoupling capacitors of 80pF, and power ground bonding wires, pads.

Fig 2. (a) Test vehicle of board (b) Test vehicle of chip
(c) Schematic of LNA (d) Schematic of mixer

Fig 3. (a) Model for the Package P/G Plane Using Balanced TLM (b) R,L,C,G table Using Balanced TLM

In order to analyze the effect of coupled digital switching noise on the performance of the RF circuits, it is important to extract precise models of on-chip and board simultaneously.

Figure 3 illustrates the model of power ground plane pair of the test board. The power ground plane of the test board was modeled as transmission line matrix method (TLM). The unit of TLM consisted of RLCG lumped components, and its size was 2mm by 2mm. The model parameter values of the unit TLM is shown in Fig 3(b). To provide stable power ground network, the model of power ground plane of test board had bulk decoupling capacitors of 20uF.

Figure 4 describes on-chip power ground models. The model parameters of the chip were extracted based on TSMC 0.25um CMOS process. Metal 2 layer was used to consist on-chip power ground network, and it contained on-chip decoupling capacitors of total 80pF. These models were designed and simulated by using Advanced Design System (ADS) and Spectre simultaneously.

(a)

Film	Rs	Unit
M1	0.076	Ω/sq
M2	0.076	Ω/sq
M3	0.076	Ω/sq
M4	0.076	Ω/sq
M5	0.041	Ω/sq

(b)

Fig 4. (a) On chip power ground model (b) Sheet resistance of on-chip metals

3. Simulation and Measurement Results of Mixer

Fig 5. Power ground self impedance curves monitored at on-chip (port 3 in Fig 2(a)); black line represents self impedance curve with on chip decoupling capacitor of 80pF, gray line shows self impedance curve without on chip decoupling capacitor, two cases have a bulk decoupling capacitor of 20uF in the test board.

Figure 5 shows simulated power ground self impedance curves monitored at on-chip power ground network of the mixer. Black curve represents self impedance with on chip decoupling capacitor of 80pF, and gray curve shows self impedance curve without on chip decoupling capacitor. Both two curves extracted from the same power ground circumstances except on-chip decoupling capacitors.

As shown in the impedance without on-chip decoupling capacitors, first inductive curve dominates the impedance plot, which comes from equivalent series inductance(ESL) of a bulk decoupling capacitor of 20uF. And a parallel resonant peak is created, which occurs between the ESL of the bulk decoupling capacitor and a board power ground capacitance at a frequency of 150MHz. Then the capacitance of the power ground cavity of the test board dominates the impedance curve. The resonant peaks in ranges at giga hertz come from multi-mode cavity resonances of the power ground plane of the test board.

However, these resonant peaks generated by the cavity mode resonances of black color curve are screened out by the impedance lowering effect of on-chip decoupling capacitors, as shown in gray color curve. A 80pF on-chip decoupling capacitors eliminate the resonant peaks over giga hertz, and it is also found that a parallel resonance is created at a frequency of 400MHz, which occur between on-chip decoupling capacitors and the ESL of power ground interconnection including bonding wires, the bulk decoupling capacitor, and the board power ground plane.

Fig 6. Power ground transfer impedance curves between port 1 and port 3 in Fig 2(a) ; black line represents transfer impedance curve with on chip decoupling capacitor of 80pF, gray line shows transfer impedance curve without on chip decoupling capacitor, two cases have a bulk decoupling capacitor of 20uF in the test board.

In Fig 6, transfer impedance curves are plotted. Black curve represents transfer impedance curve with on-chip decoupling capacitors of 80pF, while gray line shows transfer impedance curve without on-chip decoupling capacitor.

The transfer impedances show very similar trend to the self impedance plots of Fig 5. It is also found that frequencies of the resonant peaks of the transfer impedances are the same of that of the self impedances. The transfer impedance can be reduced by nearly 15dB in frequency ranges over 600MHz by using on-chip decoupling capacitors of 80pF.

However, use of on-chip decoupling capacitor could not reduce power ground transfer impedance under a frequency of 400MHz. Therefore, in order to improve the transfer impedance and reduce coupled power ground switching noise, we need to add several off-chip decoupling capacitors in RF power ground network.

In Fig. 7, we plotted transfer impedance with and without off-chip decoupling capacitors. Black curve shows transfer impedance which was extracted on power ground network with both a on-chip decoupling capacitor and two off-chip decoupling capacitors. The size of off-chip decoupling capacitors was 500nF and 100nF, respectively. In contrast, gray curves shows transfer impedance with only a on-chip decoupling capacitor.

Fig 7. Power ground transfer impedance curves between port 1 and port 3 in Fig 2(a) ; black line represents transfer impedance curve with off-chip decoupling capacitor of 20uF, 500nF, 100nF, and on-chip decoupling capacitor of 80pF, gray line shows transfer impedance curve without decoupling capacitor of on-chip decoupling capacitor of 80pF.

By using the off-chip decoupling capacitors, we can achieve a lower transfer impedance under a frequency of 100MHz, as shown in Fig 7. Consequently, we can acquire the increased performance of transfer impedance at broad frequency ranges using on-chip and off-chip decoupling capacitors simultaneously.

To verify increased performance of power ground network for decoupling capacitors, we fabricated and measured test chips and boards, which had the same structures of the proposed models in Fig 2.

Figure 8 (a) shows measured output waveforms in fabricated double balanced mixer. To compare the effect of on-chip decoupling capacitors, we intentionally added switching noise that had a frequency of 900MHz and a magnitude of 80mV_{pp} to the power ground of the test boards. As gray color waveform represents, the injected switching noise is removed by on-chip decoupling capacitors, while in the case of without on-chip decoupling capacitors the mixer output shows unwanted noise waveform. Also, the coupled noise reduction effect for on-chip decoupling capacitors is observed in frequency spectrums of the measured mixer output as shown in Fig 8 (b). When on-chip decoupling capacitor is designed to the power ground of the mixer, we can reduce coupled switching noise, which has a frequency of 900MHz, about 15dB, compared to the case without on-chip decoupling capacitor in black color spectrums.

Fig 8. (a) Measurement result of output waveform of mixer in time domain when power/ground noise generates in 900MHz (b) Measurement result of output spectrum of mixer in frequency domain when power/ground noise generates in 900MHz. gray line represents transfer impedance curve with on chip decoupling capacitor of 80pF, black line shows transfer impedance curve without on chip decoupling capacitor, two cases have a bulk decoupling capacitor of 20uF in the test board.

Figure 9 shows measured output waveform of mixer when external switching noise which has a frequency of 800kHz and a magnitude of 80mV_{pp} is injected to the power ground of the test board. We compared two cases of measured results. One is the mixer which had a on-chip decoupling capacitor of 80pF and off-chip decoupling capacitors of 500nF and 100nF. And the other is the mixer with only a on-chip decoupling capacitor of 80pF.

As observed in black color waveform, the mixer output without off-chip decoupling capacitors is coupled by external noise of a frequency of 800kHz. In the other hand, the mixer output waveform with both on-chip and off-chip decoupling capacitors shows no additional noise waveform. As seen in Fig 9 (b), coupled switching noise decreases in 15dB a frequency from 1k to 5MHz compared to the case without off-chip decoupling capacitor in Fig 9(b).

(a)

(b)

Fig 9. (a) Measurement result of output waveform of mixer in time domain when power/ground noise generates in 800kHz (b) Measurement result of output spectrum of mixer in time domain when power/ground noise generates in 800kHz. gray line represents transfer impedance curve with off-chip decoupling capacitor of 20uF, 500nF, 100nF, and on- chip decoupling capacitor of 80pF, black line shows transfer impedance curve without decoupling capacitor of on- chip decoupling capacitor of 80pF.

4. Simulation Results of LNA

In this chapter, the effect of coupled digital switching noise on the performance of LNA has been introduced using simulation results. Figure 10 shows power ground noises of LNA. When 5mV SSN noise injected to the external board, the injected noise can be reduced by on-chip decoupling capacitor of 400pF. When on-chip decoupling capacitor is designed, power ground noise at frequency of 1GHz decreases 17dB more than the case without on-chip decoupling capacitor as shown in Fig 10(b).

(a)

(b)

Fig 10. (a) Simulation Result of P/G noise waveform in Time domain for designed LNA (b) Simulation Result of P/G noise spectrum in frequency domain for designed LNA; Black line represents transfer impedance curve with on-chip decoupling capacitor of 400pF, gray line shows transfer impedance curve without on-chip decoupling capacitor.

Figure 11(a) shows simulated output waveform of the LNA.

The performance of LNA could keep well, using on-chip decoupling capacitor, as similarly to the results of the mixer. We also found that, when on-chip decoupling capacitor is designed, output waveform coupled by power ground noise at frequency of 1GHz decreases 3.5dB more than the case without on-chip decoupling capacitor as shown in Fig 11(b).

(a)

(b)

Fig 11. (a) Simulation Result of Output Waveform in Time domain for designed LNA (b) Simulation Result of Output Spectrum in frequency domain for designed LNA. ; Black line represents transfer impedance curve with on-chip decoupling capacitor of 400pF, gray line shows transfer impedance curve without on-chip decoupling capacitor.

5. Conclusion

In this paper, we have analyzed the effect of decoupling capacitors on the performance of the mixer and LNA circuits. We have incorporated models of the chip, and test board into simulations simultaneously. And we have fabricated the chip and test board, and measured the mixer output waveforms.

Power ground noise generated by the digital circuitry couples to the RF circuitry and degrades not only circuit performance but also a system performance. We verified that digital noise coupling problem can be solved as reducing the coupling noise by designing on chip decoupling capacitors and off chip decoupling capacitors simultaneously.

References

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