Parasitic S/D Resistance Effects on Hot-Carrier Reliability in Body-Tied FinFETs

Jin-Woo Han, Choong-Ho Lee, Donggun Park, and Yang-Kyu Choi

***Abstract*—Hot-carrier effects (HCEs) in fully depleted body-tied FinFETs were investigated by measuring the impact-ionization current. To understand the hot-carrier degradation mechanism, stress damages were characterized by dc hot-carrier stress measurement for various stress conditions and fin widths. The measurement results show that the generation of interface states is a more dominant degradation mechanism than oxide-trapped charges for FinFETs with a gate-oxide thickness of 1.7 nm. It was found that a parasitic voltage drop due to a significant source/drain extension resistance plays an important role in suppressing the HCEs at narrow fin widths. This letter can provide insight determining the worst stress condition for estimating the lifetime and optimizing between reliability and ON-state drain–currents.**

***Index Terms*—Hot-carrier effects (HCEs), interface states, multiple-gate FinFETs, oxide-trapped charges, parasitic source/drain (S/D) resistance.**

I. Introduction

IT IS WIDELY accepted that fully depleted multiple-gate MOSFETs will lead device scaling at the end of the International Technology Roadmap for Semiconductor (ITRS) roadmap [1]. Among multiple-gate MOSFETs, due to their simple fabrication process, ultrathin-body FinFETs are considered to be the most promising candidates for device scaling down to 10 nm [2], [3].

These devices have continuously received attention regarding hot-carrier injection (HCI) reliability [4]–[7]. These studies have made efforts in investigating the dependence of the hot-carrier effects (HCEs) on fin width $(W_{\rm Fin})$ as this is an important parameter governing short channel effects. However, the mechanisms impacting the HCEs are still under debate, as similar structures have shown different results. Some devices are more degraded [4]–[6], while others are less degraded [7] as $W_{\rm Fin}$ widens. As silicon-on-insulator (SOI) substrates have been utilized in order to fabricate FinFETs, the substrate current $(I_{\rm SUB})$ to indicate the HCEs cannot be measured due to the floating body [4], [5]. Thus, it is difficult to understand the HCEs comprehensively. The substrate current of FinFETs has been reported for the first time in bulk substrate [6]. However, further qualitative and quantitative analysis is needed in order to have a better understanding of HCEs.

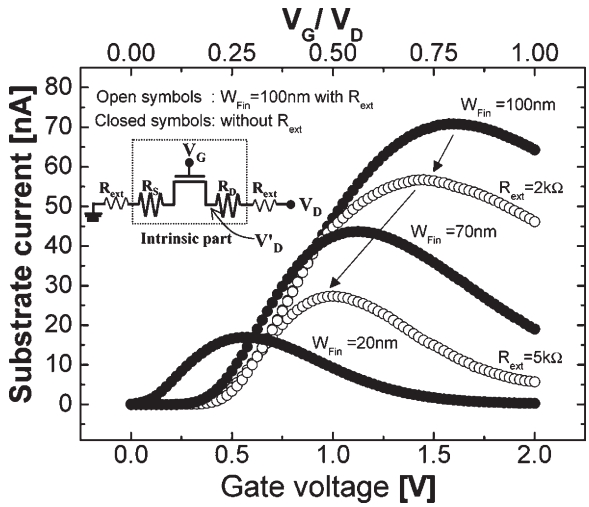

Fig. 1. Substrate current versus gate-voltage characteristics of body-tied FinFETs with/without an external resistance. The narrowing fin width of the FinFETs without an external resistor shows similar trend to the resistance increasing of $W_{\rm Fin} = 100$ nm with an external resistor. The threshold voltages were 0.2, 0.4, and 0.5 V for $W_{\rm Fin} = 20, 70$, and 100 nm, respectively.

The multiple-gate ultrathin-body devices are promising architecture due to their superior controllability for short channel effects, however, these devices can suffer from high parasitic resistance due to the narrow width of their source/drain (S/D) extension regions [8]. In this letter, focusing on the parasitic voltage drop caused by S/D extension resistance, the impact-ionization current in body-tied FinFETs was carefully characterized. And the hot-carrier degradation mechanisms and the $W_{\rm Fin}$ dependence of the HCEs were studied.

II. Results and Discussions

Body-tied FinFETs were fabricated on a bulk substrate. The fin body was directly tied to the substrate, and it was possible to measure the $I_{\rm SUB}$. In order to investigate the $W_{\rm Fin}$ dependence on the HCEs, the gate-oxide thickness $(T_{\rm OX})$, gate length (L_G), and fin height $(H_{\rm Fin})$ were fixed at 1.7, 100, and 100 nm, respectively, and the $W_{\rm Fin}$ varied from 20 to 100 nm. The fabrication process and important device parameters used in this letter were reported in [9].

The $I_{\rm SUB}$ indicating the hot-carrier generation were measured, and are shown in Fig. 1. The data showed that less impact-ionization current was observed at narrower fin width.

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This result is consistent with the previous report [6]. The multiple-gate ultrathin-body devices suffer from high parasitic resistance due to the narrow width of their S/D extension regions [8]. An increment of S/D series resistance ($R_S = R_D$) give rise to a decrease in the effective drain voltage ($V_D' = V_D - 2I_D R_S$) as well as the lateral channel field for a given external drain bias (V_D). Therefore, the drain current and the substrate current are degraded. To explain the effects of the parasitic voltage drop, extrinsic parasitic resistance ($R_{\rm ext}$) was intentionally introduced. As shown in the inset of Fig. 1, the S/D of a wide-fin FinFET was serially connected to $R_{\rm ext}$. At $W_{\rm Fin} = 100$ nm with $R_{\rm ext}$, $I_{\rm SUB}$ was decreased and the gate bias to cause peak $I_{\rm SUB}$ was lowered as the effective drain voltage [$V_D' = V_D - 2I_D(R_S + R_{\rm ext})$] was reduced with increasing $R_{\rm ext}$. The plot of $W_{\rm Fin} = 20$ nm without $R_{\rm ext}$ was expected to be similar to $W_{\rm Fin} = 100$ nm with $R_{\rm ext} = 5\,\text{k}\Omega$ corresponding to the total series resistance of $W_{\rm Fin} = 20$ nm, which was extracted by the ΔL method [10]. In the case of fully depleted thinbody FinFETs, the channel dopant could be easily diffused out and the threshold voltage (V_T) dropped as the $W_{\rm Fin}$ reduces [11]. Due to the reduction of the space charge and the vertical electric field that must be supported by the gate bias at the expense of the inversion charge, the saturation voltage ($V_{\rm Dsat}$) increased [12]. As a result of this, the plot shows that $I_{\rm SUB}$ was smaller, and the peak of $I_{\rm SUB}$ was shifted toward a lower gate voltage. The maximum electric field, expressed as $E_m = (V_D - V_{\rm Dsat})/l$ where l is a characteristic length, is useful for explaining the HCEs [13]. In order to evaluate the effect of l, $\ln[I_{\rm SUB}/I_D(V_D - V_{\rm Dsat})]$ was plotted against $1/(V_D - V_{\rm Dsat})$, then l was obtained from the slope of this line [14]. Although l is known to depend on the gate-oxide thickness and S/D junction depth, the extracted l was found to be insensitive to $W_{\rm Fin}(l \sim 29$ nm). E_m is mostly impacted by $V_D - V_{\rm Dsat}$, therefore, impact ionization was significantly lowered because V_D was decreased due to the parasitic voltage drop while $V_{\rm Dsat}$ was increased as $W_{\rm Fin}$ was decreased.

Fig. 2 shows the impact-ionization characteristics ($I_{\rm SUB}/I_D$) as a monitor of E_m [13]. There were two competing bias conditions maximizing the HCI degradation within a set operational voltage range: the intermediate gate-voltage stress for the maximum substrate current ($I_{\rm SUB\,max}$), and the high-gate-voltage stress for the maximum gate current ($I_{G\,\rm max}$) [15]. Comparing these two bias conditions, the impact-ionization rate was lowered at the high gate voltage rather than at the intermediate gate voltage, as the higher vertical field suppressed the lateral channel field. Because of the parasitic voltage drop, the measured impact ionization was monotonically reduced with the fin-width scaling. Especially in the case of the high gate bias, the higher the flow was of the drain current, the larger the drop in voltage that occurred. Therefore, $I_{\rm SUB}/I_D$ was slightly lowered at $I_{\rm SUB\,max}$ and significantly decreased at $V_G = V_D$; the discrepancy between the two conditions becomes large as $W_{\rm Fin}$ decreased. It is worthwhile to note the fact that the series resistance degraded I_D and $I_{\rm SUB}$ simultaneously. I_D is a linear function of V_D, however, $I_{\rm SUB}$ is an exponential function of V_D. Thus, for $W_{\rm Fin} = 100$ nm with external $R_{\rm ext} = 2\,\text{k}\Omega$, $I_{\rm SUB}$ decreased to 80% whereas I_D decreased to only 10% with respect to

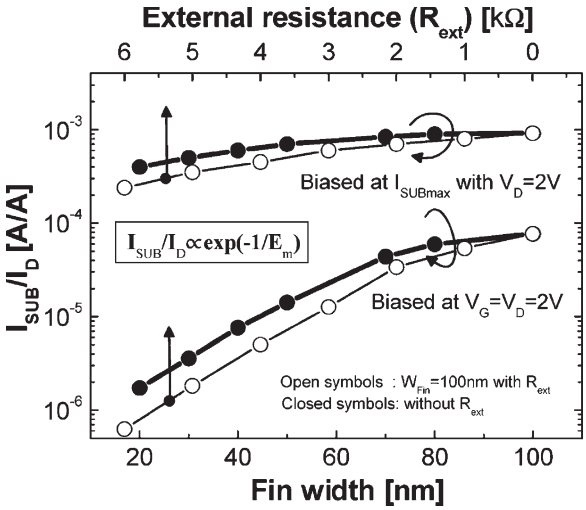

Fig. 2. Impact-ionization characteristics ($I_{\rm SUB}/I_D$) versus fin widths and external resistances. At $W_{\rm Fin} = 100$ nm with external resistance, $I_{\rm SUB}/I_D$ decreases as the external resistance increases due to a reduction of the effective drain voltage. For the same reason, the narrowing fin width shows a reduction of the effective drain voltage. The reduction of $I_{\rm SUB}/I_D$ becomes significant at the narrow fin and the $V_G = V_D$ condition.

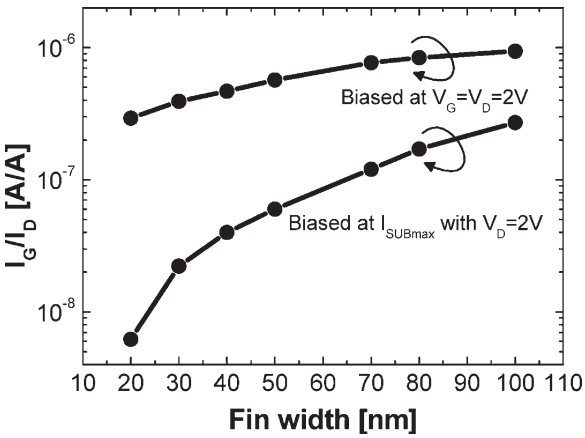

Fig. 3. I_G/I_D characteristics versus fin widths. At the condition of $I_{G\,\rm max}$, I_G/I_D increases as the fin width increases because the electric field heads for the gate oxide, and most hot carriers move towards the gate oxide. At the condition of $I_{\rm SUB\,max}$, I_G/I_D dramatically increases as the fin width increases because the gate bias causing $I_{\rm SUB\,max}$ lowers.

$W_{\rm Fin} = 100$ nm without $R_{\rm ext}$. Conclusively, an increment of the series resistance degrades $I_{\rm SUB}/I_D$.

Fig. 3 shows the gate current from the injected hot carrier for various fin widths. The device dc lifetimes are shown in Fig. 4. In the case of the $I_{\rm SUB\,max}$ stress condition, $I_{\rm SUB}/I_D$ was slightly decreased, and I_G/I_D was significantly reduced as $W_{\rm Fin}$ narrowed because the gate bias causing $I_{\rm SUB\,max}$ lowered. As a result of this, fewer hot carriers scattered with the Si/SiO_2 interface due to the lower vertical field, and less degradation occurred at the narrow fin, as shown in Fig. 4. In the case of the $I_{G\,\rm max}$ stress condition, hot carriers were strongly driven in the gate-oxide direction. This effect was more significant at wider fin having strong electric field from the gate [4], [5] and it led to increase of I_G/I_D. As higher amount of hot carriers were generated and injected into the gate oxide as

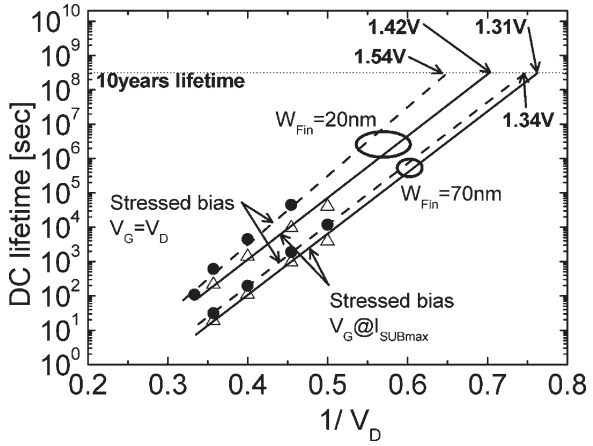

Fig. 4. DC lifetime plot extracted from a constant-voltage stress. The lifetime is defined as the time for a 10% change in the saturation current. A $I_{\mathrm{SUB}\,\max}$ bias condition degrades the device more than a $I_{G\,\max}$ bias condition, i.e., interface traps by hot electrons play a dominant role in the hot-carrier reliability. Device degradation by hot carriers is distinctly smaller at the narrow fin than at the wide fin.

W_{Fin} wideness, the wide fin FinFETs are vulnerable to HCI degradation.

It is believed that high gate current passing through gate oxide at the high gate-bias-stress results in a building up of oxide-trapped charges and a high-impact-ionization current at the intermediate gate-bias stress causes interface traps [15]. Within a given W_{Fin}, a device stressed at the $I_{\mathrm{SUB}\,\max}$ bias showed a worse HCI immunity than one stressed at the $I_{G\,\max}$ bias. Since there is insufficient room for the oxide-trapped charges to be built up due to the ultrathin gate oxide ($T_{\mathrm{OX}} = 1.7$ nm), the damage caused by the oxide-trapped charges was less crucial than that caused by interface traps [16], [17].

III. Conclusion

In this letter, the HCEs of fully depleted multiple-gate FinFETs were carefully studied for various biases and fin widths. In the ultrathin gate oxide ($T_{\mathrm{OX}} = 1.7$ nm), the generation of an interface state plays a more dominant role in hot-carrier degradation than do oxide-trapped charges. As the fin-width scales downward, the parasitic voltage drop caused by the extension series resistance results in a reduction of the hot-carrier degradation in thin-body FinFETs. Even though the parasitic series resistance can minimize the hot-carrier degradations, it should be optimized for maximizing the drive current.

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