LOW POWER CLOCK GENERATOR BASED ON AN AREA-REDUCED INTERLEAVED SYNCHRONOUS MIRROR DELAY SCHEME

Kihyuk Sung, Byung-Do Yang, and Lee-Sup Kim

Department of EECS, KAIST, 373-1 Guseong-dong, Yuseong-gu, Daejeon, Republic of Korea
E-mail: khsung@mvlsi.kaist.ac.kr

ABSTRACT

A new interleaved synchronous mirror delay (SMD) is proposed in order to reduce the circuit size. The conventional interleaved SMD has multiple pairs of forward delay array (FDA) and backward delay array (BDA) in order to reduce the clock skew. The proposed interleaved SMD requires only one FDA and one BDA by changing the position of MUX. Simulation results show that about 30% power reduction and 40% area reduction are achieved in the proposed interleaved SMD. All circuit simulations and implementations are based on 0.25 μm two-metal CMOS technology.

1. INTRODUCTION

The CPU-memory performance gap is growing larger as the time passes by. Various new memory architectures such as Synchronous DRAM, Rambus DRAM, and Double Data Rate Synchronous DRAM are proposed in order to increase the memory speed. From the viewpoint of circuit technique, phase-locked loop (PLL) and delay-locked loop (DLL) have been applied in many systems in order to suppress the clock skew [1, 2]. However, both PLL and DLL are feedback systems. At least several hundred cycles are required for both PLL and DLL to lock the system. The long lock time of PLL or DLL increases stand-by currents [3]. A recently introduced synchronous mirror delay (SMD) circuit requires only two clock cycles in order to suppress the clock skew in contrast with PLL and DLL [3-5]. An interleaved SMD circuit is proposed in order to reduce the clock skew of the SMD circuit, but the scheme increases the circuit size [4]. Recently, an analog SMD is also proposed [6-8]. However, the analog SMD is not robust to the process variations such as supply voltage and temperature.

We propose a new interleaved SMD, which uses one forward delay array (FDA) and one backward delay array (BDA) instead of multiple pairs of FDA and BDA. This paper is organized as follows. In Section 2, a review of the conventional SMD is presented. The conventional interleaved SMD is discussed in Section 3. A new interleaved SMD is proposed in Section 4. Section 5 presents simulation results. Conclusions are drawn in Section 6.

2. REVIEW OF THE CONVENTIONAL SMD

Fig. 1 shows the circuit diagram of the conventional SMD [3, 6]. Node names are given for convenience. It consists of a FDA, a BDA, a mirror control circuit (MCC), and a replica delay line of the input buffer delay d1 and the clock driver delay d2. The unit delay time (TdF) of the FDA and the unit delay time (TdB) of the BDA are equal. A clock pulse travels forward for the time of Tclk-d1-d2 through the FDA. The clock pulse is propagated backward through the BDA as it is propagated forward through the FDA. The resulting total delay time is d1 + (d1+d2) + (Tclk-d1-d2) + (Tclk-d1-d2) + d2 = 2Tclk. The clock skew is suppressed in two clock cycles. A negative pulse in E node is triggered when both B node and D node are High. In other words, the positive pulse in the external clock is inverted into the negative pulse when it is passed through the MCC. The negative pulse is propagated through the BDA. Therefore, an extra inverter is inserted in front of the clock driver in order to obtain the positive pulse. The delay of the extra inverter is negligible.

The large duty cycle of the external clock causes the FDA to detect the delay time which is smaller than Tclk-d1-d2 if the input buffer is a mere delay element of d1. In order to solve the problem, the input buffer is not only a delay element of d1 but also a short pulse generator. Therefore,
the output of the input buffer has a constant pulse width (=TON).

3. CONVENTIONAL INTERLEAVED SMD

Fig. 2. Conventional interleaved SMD

Fig. 2 shows the conventional interleaved SMD [4]. It consists of an input buffer with delay d1, a clock driver with delay d2, a replica delay line (dummy input buffer plus dummy clock driver), and a pair of delay lines (a FDA and a BDA arranged in parallel). The conventional interleaved SMD has a pair of identical delay lines in order to divide the jitter down by two. Therefore, the interleaved SMD is about two times larger than that of the non-interleaved SMD from the viewpoint of the area and the power consumption. The MUX in Fig. 2 is not a MUX but a logic gate. It is either an AND gate or an OR gate [4]. However, a real MUX is required for the interleaved SMD to operate properly.

4. PROPOSED INTERLEAVED SMD

Fig. 3. Proposed interleaved SMD

The proposed interleaved SMD is shown in Fig. 3. The proposed interleaved SMD uses one FDA and one BDA instead of two FDAs and two BDAs. Therefore, the circuit size is reduced down to a half.

An inverter is inserted in front of the clock driver in order to solve the polarity problem. Fine delay is one half of the Tpd, the unit propagation delay time of the FDA or the BDA. Dummy input buffer is required in order to find out the synchronization between the external clock and the internal clock.

Fig. 4. 2-cycle jump circuit

Fig. 4 shows the 2-cycle jump circuit in Fig. 3. Each D flip-flop is a positive edge-triggered flip-flop. It is implemented by using the true single-phase clock logic. The 2-cycle jump circuit is required because the clock synchronization between the external clock and the internal clock should be checked after two clock cycles.

Fig. 5. MUX control input generator

The control input of the MUX in Fig. 3 is generated as shown in Fig. 5. If the clock skew between the external clock and the internal clock is greater than Td (=one-fourth of Tpd), the AND gate in the MUX control input generator generates two successive pulses. And it takes two clock cycles for the internal clock to lock the external clock. Therefore, three toggle flip-flops are required at the end of the MUX control input generator. The Tend delay element (=one half of Tpd + TON) is required in order to obtain a stable MUX output signal.

The maximum clock skew is Tpd after two clock cycles. And the maximum clock skew is reduced down to a half of Tpd after four clock cycles.
5. SIMULATION RESULTS

The HSPICE simulation environment is as follows. The power supply is 2.5V and the temperature is 125°C. 0.25μm two-metal CMOS process parameter is used in the simulation.

Fig. 6 shows that the proposed interleaved SMD operates properly. The value of Tpd is 0.2nsec. The clock skew between the external clock and the internal clock is less than 0.11nsec, which is about one half of the Tpd. Power consumption is 10.18mW at 250MHz. The conventional interleaved SMD consumes as much as 16.37mW at 250MHz.

Fig. 7 shows simulation results of power consumption as a function of the supply voltage. The power consumption increases as the supply voltage increases. The power dissipation in the proposed interleaved SMD is reduced by about 30% on average compared with the conventional one.

Table 1 summarizes the above simulation results.

<table>
<thead>
<tr>
<th>Specification of the proposed interleaved SMD</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
</tr>
<tr>
<td>Supply voltage</td>
</tr>
<tr>
<td>Clock skew</td>
</tr>
<tr>
<td>Power consumption</td>
</tr>
<tr>
<td>Circuit area</td>
</tr>
</tbody>
</table>

Fig. 8 shows the jitter as a function of Tpd, the unit delay time in the proposed interleaved SMD or the conventional one. It is observed that the jitter is about one half of Tpd in the proposed double interleaved SMD. The jitter would be about one-fourth of the Tpd in the quadruple interleaved SMD [4].

Fig. 9 shows the proposed interleaved SMD is smaller than the conventional one by about 40%. The area of the conventional interleaved SMD, which has 50 delay units, is 32736μm² (48μm by 682μm) and that of the proposed one is 19318 μm² (26μm by 743μm).

Table 1 summarizes the above simulation results.
6. CONCLUSION

The proposed interleaved synchronous mirror delay requires one FDA and one BDA by changing the position of MUX. About 40% area reduction is achieved in the proposed interleaved SMD. The proposed interleaved SMD consumes less power than the conventional one by about 30%. The above two advantages over the conventional interleaved SMD are gained without degrading the jitter characteristic. The new interleaved SMD can be widely utilized as a means of clock synchronization.

ACKNOWLEDGMENT

This work was supported by KOSEF through the MICROS at KAIST, Korea.

REFERENCES


