A Large-Signal Model of RF LDMOS with Skin Effects of Power Combining Structures

Jeonghu Han¹, Changkun Park¹, Donghyun Baek², Kyoungmin Koh², Juhyun Ko², Ilhun Shon², and Songcheol Hong³

¹ Dept. of Electrical Engineering and Computer Science, KAIST, Daejeon, 305-701, Korea
² Samsung Electronics Co., Ltd., 449-71, Korea
³ * T=108°C

Abstract — An empirical large signal model is presented to have good accuracy for all the device operating regions up to 20 GHz. Skin effects of combining structures, non-reciprocal capacitance, and non-quasi-static effect are considered in this model. A power transistor of 1.92 mm gate width is modeled and compared with measured data. P1dB of 20 dBm, 19 dB gain and 62% PAE at P1dB in Pout properties are exactly predicted by the model.

Index Terms — Empirical model, large signal model, power amplifiers, power MOSFET, RF LDMOS

I. INTRODUCTION

In recent years, great effort has been directed to develop a fully integrated CMOS single-chip radio for wireless communication systems. One of the most severe parts is to implement power amplifier (PA) in CMOS due to its low breakdown voltage and hot electron effects, which necessitate an integration of RF LDMOS in CMOS process [1]. The CMOS compatibility makes it possible to integrate an LDMOS PA together with CMOS base-band and/or power control circuitry, and hence a lot of research has been done on RF LDMOS devices and circuits.

To optimize the device structure and/or to design PA circuits efficiently, an accurate model of the device becomes very important. A large-signal model over the wide range of bias conditions becomes more and more important, since modern PA topologies include a gate bias or supply voltage control scheme and variable load impedance techniques [2], [3]. Previously, RF LDMOS models utilizing the conventional MOSFET models have been reported [4]-[6]. In spite of superiority in scaling, however, the commercial models, such as BSIM3v3, have too many parameters and complex extraction routines, and practically need an additional work to extend their scalability to power transistors, which are wider than a millimeter. Another drawback is that BSIM3v3 does not support breakdown and self-heating effects [7]. From the viewpoint of an RF model, the conventional models need to be enhanced by additional circuit elements [7]. As a consequence, empirical approaches to RF LDMOS models have been proposed [8]-[10]. But, the previous models [4]-[6], [8]-[10] showed their validity for limited bias conditions and operating frequencies up to a few GHz.

In this work, LDMOS transistors for handset PAs are developed in a 0.3 μm CMOS-compatible process. An empirical large-signal model is proposed to accurately describe RF characteristics over all the device operating regions up to 20 GHz. The proposed model includes frequency dispersion effect of interconnection lines, which affects the output admittance of large transistors. A methodology is proposed to efficiently model the gate capacitances, the non-reciprocal capacitance, the source-to-drain capacitance, and the channel resistances describing non-quasi-static effect. Small-signal RF characteristics and modeling results of the LDMOS device are presented, which are followed by measured and simulated output power and power-added efficiency (PAE) data.

II. DRAIN CURRENT MODEL

The gate length of the fabricated LDMOSFETs is 0.3 μm. To obtain excellent RF power performances, the length of LDD region is set to 0.5 μm, which is shorter than those of usual LDMOSFETs. The threshold voltage is 0.57 V and the drain junction breakdown voltage is 14.1 V at zero gate voltage. The current drivability is 450 mA/mm at the gate voltage of 3.5 V. Fig. 1 shows the measured...
Fig. 2. Equivalent circuit of the proposed large-signal model.

IV. INTRINSIC DEVICE MODEL

Intrinsic capacitances were extracted from the measured Y-parameters [14] after the parasitic elements were de-embedded from the measured data. The extracted values are shown in Fig. 3 for all the measured bias conditions. The gate capacitances, $C_{gg}$ and $C_{gd}$ were modeled by the following empirical equations with 6 and 7 parameters, respectively.

$$C_{gg} = c_{g1} - c_{g2} \cdot V_{DS} - A_1 \cdot \left(1 - \tanh(c_{g3} \cdot (V_{GD} - V_{Th}))\right)$$  \hspace{1cm} (3)

where

$$A_1 = c_{g4} \left(1 - \tanh(c_{g5} \cdot V_{GST} - c_{g6})\right)$$  \hspace{1cm} (4)

$$C_{gd} = A_2 + A_3 \cdot \left(\tanh(c_{d1} \cdot \left(V_{GDOFF} - V_{Th}\right))^2 - V_{Th}\right) + 1$$  \hspace{1cm} (5)

where

$$A_2 = c_{d2} \left(1 - \tanh(c_{d4} - V_{DS})\right)$$

$$A_3 = c_{d3} \left(1 + V_{GDOFF} / c_{d5}\right)^{c_{d6}}$$

$$V_{GDOFF} = V_{ST} \cdot \ln(\exp(V_x - V_y) / V_{ST}) + 1$$  \hspace{1cm} (6)

$V_{Th}$, $V_{GST}$, and $V_{ST}$ are known parameters used in the drain current equation [10]. $C_{gs}$ is instantly derived by ($C_{gg} - C_{gd}$). $C_m$ is the trans-capacitance to represent the difference between $C_{gd}$ and $C_{sd}$ which is not implemented in the previous RF LDMOS models. The experimental result shows that $C_m$ is comparable to the other intrinsic capacitances (see Fig. 3), and hence should not be ignored. $C_{sd}$ is the source-to-drain capacitance, which affects the output capacitance. $C_{sd}$ is negative in non-saturation [15], but the previous models have not modeled this properly, and neither have BSIM3v3 [7]. In this work, $C_m$ and $C_{sd}$ were simultaneously modeled by the following equations with one fitting parameter, $\alpha$.

$$C_m = \tau \cdot g_m = \alpha \cdot C_{gs} \cdot g_m$$  \hspace{1cm} (9)

$$C_{sd} = -\tau \cdot g_{sd} = -\alpha \cdot C_{gs} \cdot g_{sd}$$  \hspace{1cm} (10)

Experimental modeling using (9) and (10) gives acceptable results as shown in Fig. 3c. Furthermore, $C_m$ and $C_{sd}$ can be efficiently implemented in the equivalent circuit at once using one current source as appended in Fig. 2. The next equation explains how the current source represents both $C_m$ and $C_{sd}$.

$$\tau \frac{dl_{DS}}{dt} = \tau \cdot \left(\frac{dl_{DS}}{dt} \cdot \frac{dv_{g}}{dt} + \frac{dl_{DS}}{dt} \cdot \frac{dv_{d}}{dt}\right)$$  \hspace{1cm} (11)

$$= \tau \cdot g_m \cdot \frac{dv_{g}}{dt} + \tau \cdot g_{sd} \cdot \frac{dv_{d}}{dt} = C_m \cdot \frac{dv_{g}}{dt} - C_{sd} \cdot \frac{dv_{d}}{dt}$$

Finally, $R_{ch}$ and $R_{chd}$ were extracted from the real parts of $Y_{11}$ and $Y_{12}$ to model the non-quasi-static effect. $R_{ch}$ and $R_{chd}$ are dependent on bias conditions, since the non-quasi-static effect arises from the distributed nature of $C_{gs}$, $C_{gd}$ and the conducting channel. From this point of view...
Fig. 3. Extracted values of bias-dependent circuit elements and modeled data computed by the proposed empirical equations at $V_{GS} = 0 - 2.4$ V and $V_{DS} = 0 - 4.8$ V. (a) $C_{gd}$ and $R_{sub}$, (b) $C_{gg}$ and $C_{gd}h$, (c) $C_m$ and $C_{sdh}$, and (d) $R_{che}$ and $R_{cheh}$.

Fig. 4. Measured and simulated $Y$-parameters at $V_{GS} = 0 - 2$ V and $V_{DS} = 2$ V, and at $V_{GS} = 0 - 4.8$ V and $V_{DS} = 2$ V. (a) $Y_{11}$, (b) $Y_{12}$, (c) $Y_{21}$, and (d) $Y_{22}$.
Fig. 6. Measured and simulated maximum stable/available gain and current gain at $V_{GS} = 0.8 - 1.6 \text{ V}$ and $V_{DS} = 4 \text{ V}$.

and by observing the extracted data, the bias dependency of $R_{ds}$ and $R_{ch}$ can be empirically expressed as functions of $C_{ds}$ and $C_{gd}$ with a few parameters (Fig. 3d):

\begin{align}
R_{ds} &= r_1 C_{gs} + r_2 (1 - \tanh(V_{DS}))(V_{GS} + r_s) \\
R_{ch} &= r_4 C_{gs} + r_5 C_{gd} + r_6 V_{DS} + r_7.
\end{align}

V. MEASURED AND SIMULATED DATA

The proposed model was implemented in Agilent's ADS. The excellent agreement between the measured and simulated $Y$-parameters (Fig. 4) indicates that the small-signal parameters were accurately modeled over various bias conditions. The frequency responses of the current and the maximum stable/available gain are presented in Fig. 5, from which $f_2$ of 40 GHz and $f_{max}$ of 25 GHz were obtained. Fig. 6 shows output power, $P_{out}$, and PAE at 900 MHz under the maximum efficiency condition. 19 dB gain and 62 % PAE were measured at 11 dB, and the same results were simulated by the model.

VI. CONCLUSION

Silicon RF LDMOS transistors were developed in a CMOS compatible process, which is used to make handset PAs. The device was modeled by the proposed empirical large-signal model, especially focused on RF performance of power combining structures. Excellent accuracy of the model was shown by the measured and simulated $Y$-parameters for wide bias conditions up to 20 GHz. Also are shown current-voltage characteristics, power-gain plots, $P_{in}$-$P_{out}$, and PAE data to be fitted very well.

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REFERENCES


