11.6 1.2Gb/s 3.9pJ/b Mono-Phase Pulse-Modulation Inductive-Coupling Transceiver for mm-Range Board-to-Board Communication

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Recently, short distance board-to-board interconnections are widely employed in portable systems and wearable devices to accommodate many components into an extremely tight footprint. In particular, portable devices such as smart phone and tablet require over 1Gb/s data transfer through ~1mm distance between AP board and a high resolution wide screen display board. Most of display interfaces are implemented with wire-line F-PCB connector, but, they suffer from: 1) high manufacturing cost, 2) the large form factor of the connector and standard socket and 3) large capacitance values of the connector and socket degrading the channel characteristics. So far, various communication interfaces have been tried to realize low cost, small form factor and low energy operation, but with limited success. The bi-phase pule modulation was used in board-to-board communication rather than base-band transmission due to its low energy operation [1-5]. This method used the positive pulse current for data '1' and the negative pulse current for data '0', and the receiver recovered the data by sampling the data at the exact time, which requires an accurate delay control unit. However, the bi-phase pulse modulation consumes significant power because: 1) current pulses sampled at every data consume large current in TX, and 2) a power hungry delay control unit is required to exactly control the sampling time.

An ultra-low power mono-phase inductive coupling interface is presented with small form factor and high data rates (Fig. 11.6.1). Its mono-phase modulation can reduce the number of current pulses by half (average) in TX and its asynchronous demodulator can remove the power hungry delay control unit in RX. In addition, the injection-locking ring oscillator can recover the clock signal with low energy consumption. Thanks to these three low energy schemes, the data transceiver and the clock transceiver consume only 3.9pJ/b and 0.73pJ/b, respectively, for 1mm distance board-to-board communication.

Figure 11.6.2 shows the operation of the proposed mono-phase pulse modulation data transceiver. The data '1' is modulated to the mono-phase pulse and the data '0' is not sampled at all, which reduces in average 50% energy of the previous bi-phase pulse modulation. The receiver front-end receives the differentiated pulse and converts to the mono-phase pulse signal by amplifying and hysteresis comparison operation. Then, the clock asynchronous demodulator recovers the original data with a simple pulse detection logic composed of a Toggle switch, 2 FFs and a XOR gate. The pulse detection logic does not need a clock control sequence leading to significant power saving.

Figure 11.6.3 shows the circuit diagram of proposed mono-phase pulse modulation transceiver. Since the pulse width has a strong relationship with the power consumption and the BER, the mono-phase pulse generator generates pulse widths from approximately 300ps to 620ps, adaptively, for various channel conditions. Figure 11.6.3 shows the measurement results of the power consumption and BER as a function of pulse width. When the pulse width is < 560ps, the ISI caused by inductance degrades the BER rapidly. From Fig. 11.6.3, 560ps is the most energy efficient pulse width under 10^{-11} BER. The RX front-end shown in Fig. 11.6.3 is composed of two current mode logic (CML) amplifiers and one digitizer circuit. First CML amplifier in the RX front-end amplifies the small RX input signal and the second CML amplifier works as the hysteresis comparator. Since the output of the second CML amplifier does not have rail-to-rail swing, a latch is employed to ensure the full-swing pulse data with PVT variation. Each CML amplifier consumes 0.65mW and the latch consumes 0.31mW. The proposed RX front-end has 63mV sensitivity at 1.2V supply voltage. Figure 11.6.3 shows the low-energy flip-flop circuit. The MOS M_1 and M_2 are inserted to reduce the precharge voltage. The V_{DD}-V_{th} rather than V_{DD} precharge voltage reduces the energy consumption by 17% at the 1.2Gb/s data rate.

Figure 11.6.4 shows the clock transceiver and its measurement results. The receiver is composed of the inverter-based amplifier with 20KΩ feedback resistor and injection-locking ring oscillator (ILRO) with tunable current source [6]. The ILRO can recover the clock signal with only small input swing voltage, thus relaxing hardware requirements and leading to low energy consumption in the transceiver. Figure 11.6.4 shows the spectrum waveform of the receiver output. The 1.09GHz free running frequency is locked to the 1.2GHz clock frequency as the injection-locking occurs. The measured locking range is from 1.02 to 1.36GHz at room temperature. Figure 11.6.4 also shows the recovered clock eye diagram with 2.2ps RMS jitter.

Figure 11.6.5 shows measured channel characteristics of the proposed inductive coupling interface including time domain waveforms of data recovery and BER as a function of data rate. The left waveform of Fig. 11.6.5 shows the data recovery waveforms with 1.2Gb/s 2^{31}-1 PRBS data input. The input data is modulated to the mono-phase pulse and successfully recovered. The right graph of Fig. 11.6.5 shows the BER as a function of data rate and its BER rapidly increases over 1.2Gb/s. The measured RX sensitivity is 63mV and the maximum communication distances and the misalignment of inductor channels are ~1mm and ~0.7mm, respectively.

Figure 11.6.6 shows the performance comparison graphs and table for data transceivers and clock transceivers. The transceiver with lower FOM shows better energy efficient performance. The left graph of Fig. 11.6.6 shows the FOM of data transceivers as a function of the communication distance. Most of the previous works [2-5] were for the tens of micrometers range and only [1] for mm-range communication distance. In general, the delay control unit consumes tens of mW, but [1] does not include the power consumption of the delay control unit which needs 2ps resolution. The right graph of Fig. 11.6.6 shows the FOM of the clock transceivers as a function of communication distance. The ILRO based clock transceiver leads to the best FOM even with small ratio of inductor area and communication distance. Fig. 11.6.6 compares the performance of the proposed transceiver and previous works. The proposed work shows the best performance in the application to the mm-range communication.

Figure 11.6.7 shows the chip micrograph and performance summary. The test chip is fabricated UMC 130nm CMOS. The die area is 2,320um x 2,320um and the data rate is 1.2Gb/s. The data transceiver consumes 4.7mW and clock transceiver consumes 1.75mW at a supply voltage of 1.2V. The energy consumption of the data transceiver is 3.9pJ/b which is the lowest energy consumption reported to date for mm-range board-to-board communication. Low energy data transfer from AP to a wide screen HD display of a smartphone is successfully demonstrated with this chip.

Acknowledgements:
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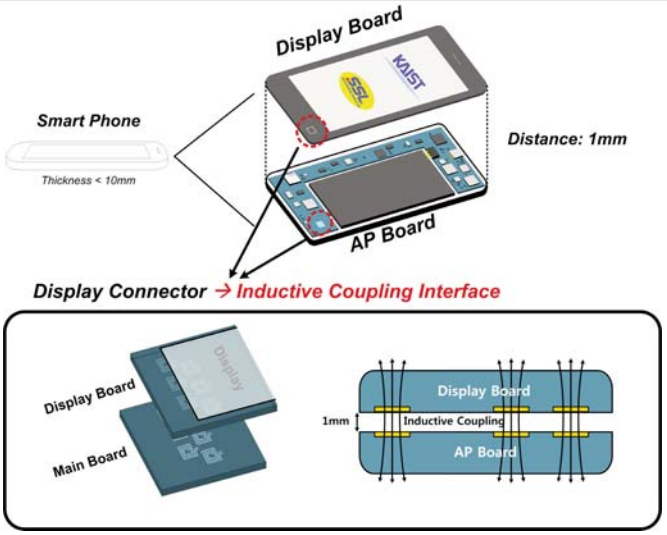


Figure 11.6.1: Proposed inductive coupling interface between AP board and display board in mobile devices.

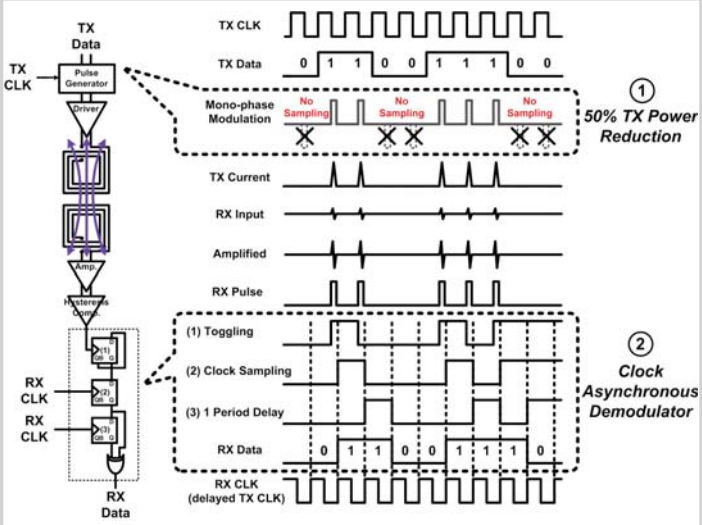


Figure 11.6.2: Data recovery flow of mono-phase pulse modulation data transceiver.

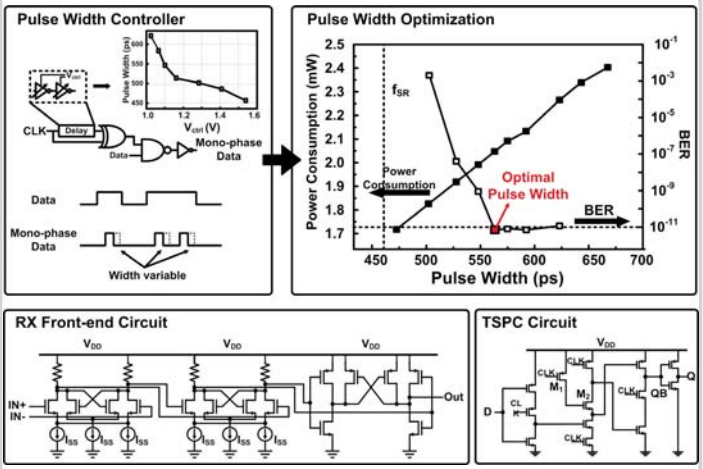


Figure 11.6.3: Data transceiver circuits including width controllable pulse generator, RX front-end, and low energy TSPC.

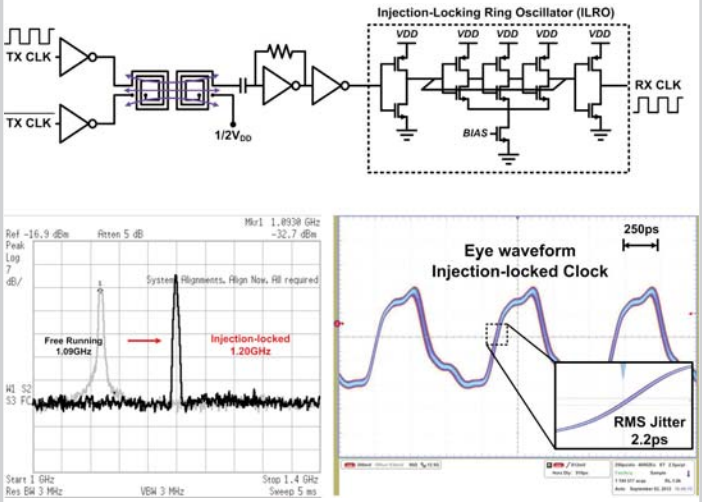


Figure 11.6.4: Clock transceiver using the injection-locking ring oscillator and measurement results.

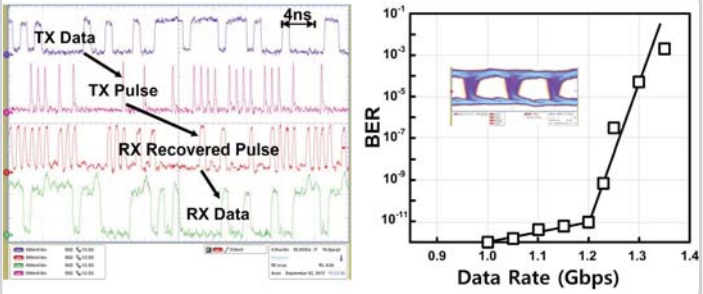
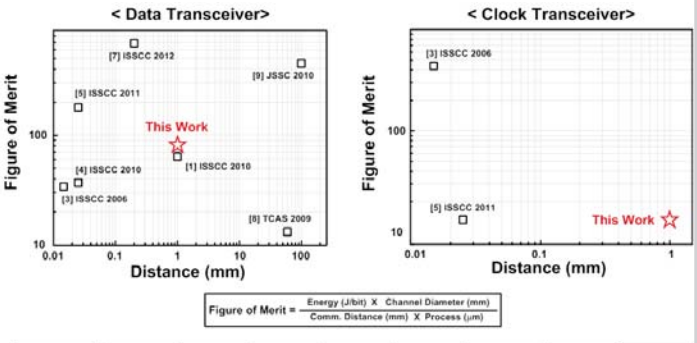
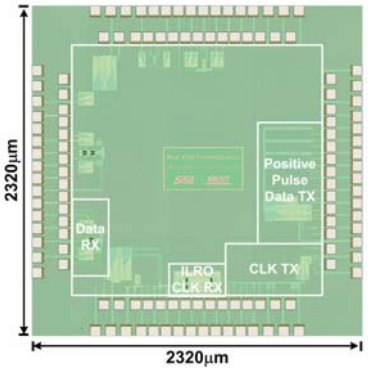


Figure 11.6.5: Waveforms of data recovery flows and BER with the data rate.



Parameters	[1] ISSCC 2010	[3] ISSCC 2006	[4] ISSC 2010	[5] ISSCC 2011	[7] ISSCC 2012	[8] TCAS 2009	[9] JSSC 2012	This Work
Process	90nm	180nm	65nm	180nm	90nm	250nm	65nm	130nm
Channel	Inductor	Inductor	Inductor	Inductor	Transmission Line	Inductor	Antenna	Inductor
Comm. Distance	1mm	15mm	25μm	25μm	200μm	6cm	10cm	1mm
Channel Size	1mm x 1mm	30μm x 30μm	60μm x 60μm	900μm x 900μm	0.4mm x 5mm	1cm x 1cm	1cm x 1cm	2.4mm
Data TRX Energy	6pJ/b	3pJ/b	1pJ/b	0.8pJ/b	8.88pJ/b	20pJ/b	290pJ/b	3.9pJ/b
Clock TRX Energy	x	1.5pJ/b	x	0.1pJ/b	x	x	x	0.73pJ/b

Figure 11.6.6: Comparison graph and table for data/clock transceivers.



Technology		UMC 130nm RF CMOS
Die Area		2320μm x 2320μm
Inductor Size		2.4mm x 2.4mm
Communication Distance		1mm
Speed		Data: 1.2Gb/s, Clock: 1.2GHz
BER		10^{-11} (2^{31}-1 PRBS Data)
Supply Voltage		1.2V
Signaling		Mono-phase Pulse Modulation
Power Break-down	Data Transceiver	
	Pulse Generator	0.69mW
	Current Driver	1.78mW
	RX Amp.	1.61mW
	Demodulator	0.62mW
	Total	4.7mW
	Clock Transceiver	
	Current Driver	0.97mW
	ILRO RX	0.78mW
	Total	1.75mW

Figure 11.6.7: Chip micrograph and its performance summary.

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