The Impact of Semiconductor Technology Scaling on CMOS Radio

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Abstract: The impact of nm CMOS technology on the various RF circuit components such as active, passive and digital circuits are presented. Firstly the impact of scaling on the LNA noise and linearity is thoroughly analyzed for the active circuits. Then two new circuits inventions named CCPP (CMOS Complementary Parallel Push-pull) circuit and the use of parasitic V-NPN (Vertical-NPN) bipolar transistor for DCR (Direct Conversion Receiver) are introduced. In CCPP, the high RF performance of PMOS comparable to NMOS, provides single ended differential RF signal processing capability without the use of balun. The use of parasitic V-NPN (Vertical-NPN) bipolar transistor, available free in triple well CMOS technology, has shown to provide more than an order of magnitude improvement in LNA noise and DC offset related problems, which have been the bottleneck for CMOS single chip integration. Then CMOS technology scaling for various passive devices, performance scaling for the inductor, variable capacitors, MIM capacitor, and switched capacitor, are discussed. Both the forward scaling of the active layer as well as the inverse scaling of interconnection layer, i.e., more interconnection layers with effectively thicker total dielectric and metal layers, provide very favorable scenario for all passive devices. Finally the impact of CMOS scaling on the various digital circuits are analyzed, taking the digital modem blocks, on the various digital calibration circuits, on the switching RF power amplifier, and eventually on the software defined radio, as examples.

Key words: nm CMOS, RF CMOS, Integrated passives, Wireless digital circuits, Digital calibration

1. Introduction

Recently we have seen widespread of various mobile computing and communication services. It is expected that total wireless market become larger than wired one from 2005. The driving force for this is the low cost and low power consumption provided by the never-ending semiconductor technology scaling. Therefore it is now time to see how the semiconductor technology scaling influences future wireless circuit and system. In Sec. 2, impact of active device scaling on RF active circuits as well as transceiver architectures will be introduced. Then impact of technology scaling on various passive devices will be discussed in Sec. 3, which is as important as active ones. In Sec. 4, the impact of device scaling for digital circuits will be illustrated, followed by conclusion.

2. Impact of Active Device Scaling on RF Active Circuits and System

The simplicity of the following MOSFET drain saturation current equation has contributed greatly to IC technology.

\[
I_{dsat} = \mu C_{\text{gs}} W / L (V_{gs} - V_{th})^2. \tag{1}
\]

In scaled CMOS technology, due to the mobility degradation by vertical as well as lateral electric fields, (1) reduces to the following simple equation with reasonable accuracy,

\[
I_{dsat} \approx W K (V_{gs} - V_{th}). \tag{2}
\]

(2) states that \( g_m \) is constant independently of channel length as well as gate drive. In RF circuit, the impedance level should be determined at \( Z_0 \) of 50 Ohm. Thus transistor width is chosen to obtain desired impedance level. Once transistor width is chosen, we obtain following scaling rule.

\[
C_{gs} \sim \lambda, f_f = 1/\lambda, f_{\text{max}} \sim 1/\lambda \tag{3}
\]

Here \( \lambda \) is the technology-scaling factor. According to the Fukui [1], minimum noise figure of a FET can be expressed as

\[
NF = 1 + K f / f_f - 1 + K_f \gamma \tag{4}
\]

(4) states that \( NF \) scales as \( \lambda \) in dB scale, which is verified as shown in Fig. 1. In low noise amplifier circuit, as input matching is deviated from noise optimum point, noise figure increases as follows.

\[
NF = NF_{\text{min}} + R_n / G_{s} \{(G_{s} - G_{s,\text{opt}})^2 + (B_{s} - B_{s,\text{opt}})^2\} \tag{5}
\]

Here we can see easily that \( R_n = \lambda, G_{s,\text{opt}} = 1/\lambda, \) and \( B_{s,\text{opt}} = 1/\lambda \), which indicates matching becomes tougher by \( 1/\lambda \) times, while the noise circle becomes broader by \( 1/\lambda^2 \) times. This makes LNA circuit design much easier. One of the insensitiveness is shown in Fig. 2, which
shows that NFmin for scaled CMOS has much less sensitivity on the gate bias. Especially the decrease of the noise resistance $R_n$ as shown in Fig. 3 helps greatly to the insensitiveness.

Linearity of RF circuit is another important circuit performance parameter for digital radio. In RF CMOS, most of the non-linearity is due to that in the transconductance. Fig. 4 shows second derivative of MOS transconductance, and IIP3 calculated based on this is also shown in Fig. 5 and Fig. 6, respectively. As can be seen, IIP3 scales adversely. However, there are many ways to improve this for scaled CMOS circuits using various negative feedback, by trading-off with other circuit parameter such as gain, for example [3].

In CMOS technology, NMOS is mostly used for RF application due to its superior performance. In scaled CMOS, however, PMOS as well as parasitic vertical bipolar transistor (V-NPN) available in deep triple well, also show good RF performance, too, as shown in Fig. 7. As results, PMOS combined with NMOS, can be used as push-pull RF circuits as shown in Fig 8 [4]. In push-pull CMOS RF circuits, highly symmetric differential circuit action is feasible without the use of bulky balun, providing very good IIP2 performance as well as large isolation. Our experimental results show more than an order of magnitude improvement in IIP2 and various isolation performances. On the other hand, V-NPN provides very low 1/f noise as well as low DC offset as shown in Fig. 9 and 10, respectively, both of which can open new horizon for direct conversion receiver [4]. Fig. 11 shows how the frequency limitation of V-NPN can be overcome by employing novel architecture such as single IF one.

3. Impact of CMOS scaling for passive devices

In CMOS scaling, both active devices as well as lowest interconnection line scale down, which is called forward scaling. However, top level metallization scales inversely, in other word, top metal thickness becomes thicker as well as total dielectric insulator thickness becomes thicker. These combined with better transistor scaling, therefore, will lead all the passive devices performance to scale favorably. For example, inductor will have better quality factor, coupling MIM capacitor will have smaller parasitic capacitance to substrate, varactor’s quality factor will be better, and switched capacitor will have much better quality factor, all in favorable direction. Detailed prediction on these performances will be presented at the workshop.

4. Impact of CMOS scaling for digital circuitry

Because digital signal processing provides inherent accuracy (6dB/bit and ppm accuracy of clock), adaptability, flexibility, and programmability, we see more and more digital circuitry in modern radio. These allow us, sophisticated signal processing (selectivity and sensitivity up to Shannon’s limit), and auto calibration (trimming) for RF/IF/BBA analog circuit imperfections, and so forth. Figure 12 shows how Moore’s law helps us obtain Shannon’s limit with affordable power consumption in hand held phone. One example for digital trimming for the analog circuit imperfection is shown in Fig. 13. The unique advantages of CMOS technology is that it is the only technology that provides all of the imperfection measurement, correction algorithm, and correction, and correction data storage device and circuitry in a same chip. As a result, trimming can be done very cheaply, which used to be done by costly labor. More examples on digital use for future radio will be presented at the workshop.

5. Conclusion

Endless scaling of modern semiconductor technology has changed mobile hand held radio system and service drastically during last two decades. Soon everyone carries billions of transistors in his mobile information terminal consuming only few hundreds of milli-watt. In this presentation, we showed that technology scaling helps continuously for us to get more smart system in less expensive way. We will see all digital except RF LNA, mixer, and RF filter in near future radio, and someday, we will have all digital radio except LNA and ADC, such as ideal software radio and ultra-wide band transceivers, where everything will be defined by software exactly as the personal computer at present.

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References


Fig. 1 NFmin vs. channel length.

Fig. 2 NFmin vs. gate-to-source bias voltage.

Fig. 3 Noise resistance, $R_n$ vs. channel length.

Fig. 4 $g_m$ vs. gate-to-source bias voltage.

Fig. 5 $I_{IP3}$ vs. gate-to-source bias voltage.

Fig. 6 $I_{IP3}$ vs. inverse channel length.

Fig. 7 State-of-the-art transistor performance.
Fig. 8 Complementary CMOS parallel pushpull amplifier schematic diagram [3].

Fig. 9(a) FFT mixer

Fig. 9(b) V-NPN mixer

Fig. 10 V-NPN mixer gives an order of magnitude improvement in DC offset [4].

Fig. 11 Single-IF DCR receiver using V-NPN in second mixers.

Fig. 12 CMOS scaling contributes greatly to obtain Shannon's limit for mobile phone with affordable power consumption.

Fig. 13 (a) Digital trimming of VCO coarse frequency (a) and fine IF filter characteristics (b) [5].