Quantum-Well Doped p-Channel AlGaAs/GaAsSb/AlGaAs Heterostructure Field-Effect Transistors

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Abstract—We report the first quantum-well doped p-channel AlGaAs/GaAsSb/AlGaAs heterostructure field-effect transistor (HFET) with 50-μm gate length and 400-μm gate width. Using a simple analytical model, we obtain accurate values of the low-field hole mobility, threshold voltage, parameters characterizing the gate leakage current, and the saturation currents and voltages. The calculation results are in good agreement with the experimental data.

The maximum transconductance in p-channel HFET's is primarily limited by its gate leakage current [1] related to a relatively small valence-band discontinuity. It is expected that an AlGaAs/GaAsSb/GaAs heterostructure has a deeper quantum well than an AlGaAs/InGaAs/GaAs structure [2], which may alleviate the gate leakage current problem. In this brief, we present the results of a study of quantum-well doped p-channel AlGaAs/GaAsSb/GaAs HFET's with 50-μm gate length and 400-μm gate width. We compare the measured data with the calculated results based on a simple long-channel HFET model.

A schematic cross section of quantum-well doped p-channel AlGaAs/GaAsSb/GaAs HFET is shown in Fig. 1 [3]. The growth was performed on (100) semi-insulating GaAs substrates in a Varian 360 MBE system at a substrate temperature of 580°C. After surface preparation, a 1-μm GaAs buffer layer was grown. The growth rate was 0.23 nm/s, and the Si-doping concentration was 1 × 10^{15} cm^{-3}. The growth was continued by the deposition of a 20-nm GaAsSb layer with 15% GaSb content and Be-doped with a concentration of 4 × 10^{18} cm^{-3}. The lattice mismatch between GaAsSb, containing 15% GaSb, and GaAs is approximately 1%. It is expected that this film is grown as a strained layer since its thickness is only 20 nm. The growth rate was 0.23 nm/s. The barrier layer of semi-insulating AlAs/GaAs was then grown at a rate of 0.328 nm/s to a thickness of 30 nm. Finally, a layer of GaAs for ohmic contact was grown with Be-doping concentration of 4 × 10^{19} cm^{-3}. This growth was accomplished at a rate of 0.115 nm/s to a thickness of 50 nm. The structure was defined using optical lithography methods with a contact aligner. After the structure growth detailed above, mesa isolation was accomplished using a hydrofluoric acid/hydrogen peroxide solution to etch through to the buffer layer. Source and drain patterns were then photolithographically defined, and layers of Au/Zn/Au were sequentially evaporated for ohmic contacts. The wafers were annealed at 370°C for 10 s. Following the anneal, gate patterns were photolithographically defined. A gate recess was performed using an ammonium hydroxide/hydrogen peroxide-based solution. Source-drain saturation current was used to monitor the recess etching depth. Finally, Al was evaporated as the Schottky gate metal and patterned using a metal lift-off technique. The measured device characteristics are shown in Figs. 2-4 where they are compared with the results of our calculation.

In our calculation, we use an empirical equation for the drain-to-source current below saturation

\[ I_d = \frac{qW\mu_0}{L_G} \left[ P_s V_{ds} - \frac{V_{ds}^2}{2a(1 + 2nV_{th}/aP_s)} \right] \]  \hspace{1cm} (1)

As shown in [4], this equation is in excellent agreement with an exact numerical calculation based on our unified charge-control model [5]. The two-dimensional gas (2-DHG) density at the source contact is related to the gate voltage as follows:

\[ V_{gs} - V_T = \eta V_{th} \ln \left[ \frac{P_t}{P_0} \right] + a(P_s - P_t) \]  \hspace{1cm} (2)

Here, \( V_{gs} \) is the gate-to-source voltage, \( V_T \) is threshold voltage, \( P_s \) is the 2-DHG density at source side in the channel, \( \eta V_{th} \) is the inverse slope of the logarithm of the subthreshold current variation with gate voltage, \( V_{th} \) is thermal voltage, \( a = g_0 \Delta d/\epsilon_s \), \( \Delta d \) is the thickness of the AlGaAs layer, \( \epsilon_s \) is a dielectric constant of GaAs, \( \epsilon_t \) is a dielectric constant of AlGaAs, \( \alpha \) is the effective distance of the 2-DHG from heterointerface to charge centroid (\( \approx 45 \AA \)), \( P_0 \) is the 2-DHG density at threshold (\( \approx 5 \times 10^{17} \text{ cm}^{-3} \)), \( L_G \) is the nominal gate length, and \( \mu_0 \) is a low-field hole mobility.
In the strong inversion regime, \(2qV_{DS}/aP_t \ll 1\) and (1) reduces to the conventional Shockley model. For the threshold regime \((2qV_{DS}/aP_t \gg 1)\) and very small drain bias \((qV_{DS} \gg V_o)\), (1) reduces to \(I_{ds} = (aW_0/L_0)P_tV_{DS}\) as it should be. The saturation voltage can be found from the condition \(\partial I_{ds}/\partial V_{DS} = 0\) which leads to \(P_t = V_{ds(th)}/a(1 + 2qV_{DS}/aP_t)\), where \(V_{ds(th)}\) is the drain saturation voltage. In the strong inversion regime \((2qV_{DS}/aP_t \ll 1)\)

\[
V_{ds(th)} = aP_t, \tag{3}
\]

and

\[
I_{ds(th)} = (qW_0/2L_0) aP_t^2, \tag{4}
\]

as expected. In the subthreshold regime, \(V_{ds(th)} = 2qV_{DS}\) and \(I_{ds(th)} = (qW_0/L_0) qV_{DS}/aP_t\) as it should. Hence, our model describes the entire range of gate voltages from below to above threshold (see [6] for more details).

Up to now, we neglected the gate leakage current which increases substantially at large gate bias and leads to reduction of drain current (i.e., negative transconductance) [7]. The gate-to-source and gate-to-drain currents are calculated using the modified diode equations

\[
I_{gs} = I_o \left[ \exp \left( \frac{V_{gs} - \eta_1 V_{th} - \eta_2 I_{gs}}{m V_{th}} \right) - 1 \right] \tag{5}
\]

\[
I_{gd} = I_o \left[ \exp \left( \frac{V_{gs} - \eta_1 V_{th} - \eta_2 I_{gd}}{m V_{th}} \right) - 1 \right] \tag{6}
\]

where \(I_o\) is a diode saturation current, \(m\) is an ideality factor, \(\eta_1\) and \(\eta_2\) account for the distributive nature of the gate current, and \(R_e\) is a linear slope of \(I_{gs}\) at high gate bias. Then, the extrinsic drain current and extrinsic gate-to-source voltage are found from \(I_{DS} - I_{D0} - \alpha G(I_{GS} - I_{D0})\) and \(V_{DS} = V_{GS} + R_e(I_{DS} + I_{D0})\) where \(\alpha G\) is a factor of the drain current reduction caused by the gate current.

We use a unified and ambigious way to determine the HFET saturation currents and voltages which has been successively applied to n-channel HFET's \((L_C = 1-5 \mu m)\) [8]. The saturation currents and voltages are experimentally determined by the differentiating the output drain resistance (see [8] for further details). In the plot of the output drain resistance, \(r_{DSS}\) versus drain voltage, the linear portion of the \(r_{DSS}\) curve indicates the transition region between linear and saturation regions

\[
r_{DSS} = \frac{\partial V_{DS}}{\partial I_{DSS}} = \frac{\lambda}{I_{DSS} - V_{DSS(th)}} [V_{DS} - V_{DSS(th)}]. \tag{7}
\]

Here, \(I_{DSS}\) is the drain-to-source current and \(\lambda\) is a characteristic length for channel length modulation [6], [8]. Equation (7) accounts for a finite output conductance in the saturation region. The determined saturation points are shown in Fig. 1.

From (2)-(4) for the strong inversion regime, we obtain

\[
G_{DSS(th)} = \frac{\partial I_{DSS(th)}}{\partial V_{DSS(th)}} = \frac{qW_0}{2aL_0} [V_{GS} - V_{T1}] \tag{8}
\]

Equation (8) allows us to extract the value of the low-field mobility and threshold voltage (see Fig. 1). The slope of the least square fitting curve is directly proportional to the low-field mobility. The measured slope is given by

\[
\text{Slope} = \frac{\partial G_{DSS(th)}}{\partial V_{DSS}} \approx \frac{qW_0}{2aL_0} = 7.14 \times 10^{-3} [\text{A/V}^2] \tag{9}
\]

leading to \(\mu_0 \approx 56 \text{ cm}^2/\text{V} \cdot \text{s}\). Here, \(a/q = 1/C_{GS} = 1/C_1 + 1/C_2 = d_{gd}/\epsilon_2\) where \(C_2 = \epsilon_2/d, C_1 = \epsilon_1/\Delta d, \) and \(d_{gd} = d + \)
(ε_f/ε_o) Δd. In our devices, d = 300 Å and d_g = 342 Å. An accuracy of the low-field mobility ρ is substantially influenced by the precise determination of the AlGaAs layer thickness d. We can also deduce the low-field hole mobility from the slopes of I_d/β-V_g. 

At positive gate bias, our devices are not fully pinched off. The drain leakage current at positive gate bias increases from ~0.2 μA at V_g = −0.1 V to ~2 μA at V_g = −1 V. In our calculation, this leakage current was added to the intrinsic drain current. We used the following parameter values: ρ = 56 cm²/V · s, β = 0.7 V, L = 9.4 nA, m = 1.4, α = 0.15, k_1 = 0.1, k_2 = 1.1, R_g = R_g = 400 Ω. Figs. 2–4 show the comparison between measured and calculated I-V characteristics, drain and gate currents, and transconductance, respectively. The calculation results are in good agreement with the experimental data.

We also calculated the hole mobility in GaAsSb using a computer program and material parameters given in [9]. The calculated values are on the order of 350 cm²/V · s, much greater than the deduced values of hole mobility. One possible explanation is the presence of large dislocation density in the channel. Our calculation shows that the dislocation density on the order of 10⁸ cm⁻² is required to reduce the hole mobility to such low values.

In conclusion, we fabricated the first quantum-well doped p-channel AlGaAs/GaAsSb/GaAs HETF's with 50-μm gate length and 400-μm gate width. The calculation results based on a simple analytical model are in good agreement with the experimental data. From the device data, we deduced the low-field hole mobility close to 60 cm²/V · s at room temperature, which is much lower than expected. We obtained the gate turn-on voltage of ~0.37 V, which is also much lower than expected. Hence, further improvements in material quality of the AlGaAs/GaAsSb/GaAs material system are required in order to improve the device performance.

References


Rapid Electrical Measurements of Back Oxide and Silicon Film Thickness in an SOI CMOS Process

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Abstract—We propose to use the front and the back gates of a fully depleted SOI transistor to extract the thickness of both the silicon film and the buried oxide, by plotting the variation of the threshold voltage of the transistor driven by one gate versus the bias on the other gate and vice versa. This allows to derive independently both the silicon film and the buried-oxide thicknesses.

I. INTRODUCTION

SOI can now be used in VLSI CMOS processes. It uses its isolation properties, due to the buried oxide below the active silicon film. Compared to bulk-Si CMOS processes, in SOI CMOS, both the buried oxide (t_ox) and silicon film (t_sil) thicknesses must be known in addition to the process parameters such as the gate oxide and the well doping, in order to characterize the completed process. An electrical method was proposed in [1] which uses a five-terminal device. The two extra terminals are the back gate and a body contact which is a lateral contact to the SOI film under the gate area. This last terminal demands a special test structure and is difficult to use in submicrometer devices, owing to the access resistance increase.

We propose a method using the back gate in addition to the three common MOS etrodes. No special design is needed: any fully depleted SOI transistor can be used. It is applied to two materials (ZMR and SIMOX).

II. THEORETICAL FORMULATIONS

SOI MOS transistors are easy to describe with a one-dimensional (1D) model, when they are fully depleted [2]. A coupling exists then between the front and the back gate. This is accomplished when t_ox < 2 W_{max}, where W_{max} is the maximum depletion layer width in the silicon. When this is fulfilled, we can use [2, eq. (12)]. Neglecting the back interface traps reads

\[ V_f' = V_f + \frac{Q_d}{C_{ox}} - \left( V_f - V_{fb} - 2\phi_b + \frac{Q_d}{C_{ox}} \right) \]

\[ \frac{C_{ox}}{C_{ox} + C_b} \]

where

\[ V_f', V_{fb}, V_f, \frac{Q_d}{C_{ox}} \]

front threshold and back gate voltages,

\[ \frac{C_{ox}}{C_{ox} + C_b} \]

front- and back-gate oxide and depletion area capacitances,

Q_d

deployed film charge density.

Let us derive (1) with respect to V_f'.

\[ \Delta V_f' / \Delta V_f = \frac{C_{ox} + C_b}{C_{ox} + C_b} \]

\[ \frac{C_{ox}}{C_{ox} + C_b} \]

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