Current-Voltage and Capacitance-Voltage Characteristics of Modulation-Doped Field-Effect Transistors

KWIYRO LEE, STUDENT MEMBER, IEEF, MICHAEL S. SHUR, SENIOR MEMBER, IEEF, TIMOTHY J. DRUMMOND, AND HAEIS MORKOC, SENIOR MEMBER, IEEF

Abstract—A model describing \( I-V \) and \( C-V \) characteristics of modulation-doped FET's is developed and used to predict the performance of Al\(_x\)Ga\(_{1-x}\)As/AlAs FET's in good agreement with our experimental results. It is shown that the change in the Fermi energy with the gate voltage changes the effective separation between the gate and the two-dimensional electron gas by about 80 \( \AA \). Current-voltage characteristics were calculated using a two piece as well as a three piece linear approximation for the electron velocity and compared with experimental results. At 300 K, the two piece model overestimates the current predicted by the three piece model only by approximately 10–20 percent. At 77 K, however, the three piece linear approximation for the velocity field characteristic should be used since the electron mobility decreases very abruptly at about 200 V/cm. The effect of the nonlinear source resistance is also discussed along with the gate-source and gate-drain capacitances, parameters of paramount importance in determining device performance. These capacitances are calculated as functions of gate-to-source and drain-to-source voltages below saturation.

LIST OF SYMBOLS

- \( a \) : Slope of the linearized \( E_F(n_e) \) function.
- \( C_{gd} \) : Gate-to-drain capacitance.
- \( C_{gs} \) : Gate-to-source capacitance.
- \( d_s \) : Thickness of undoped (Al, Ga)As at the heterointerface.
- \( d_d \) : Thickness of doped (Al, Ga)As beneath the gate.
- \( d_t \) : Total thickness of (Al, Ga)As beneath the gate.
- \( \Delta d \) : Correction for gate metal to a two-dimensional electron gas spacing.
- \( D \) : Two-dimensional density of states (3.24 \( \times \) 10\(^{17} \) m\(^{-2} \) V\(^{-1} \)).
- \( \Delta E_c \) : Conduction band discontinuity at the heterojunction.
- \( \Delta E_{F0} \) : Zero intercept of the linearized \( E_F(n_e) \) function.
- \( E_0 \) : Energy of the first subband in the triangular well.
- \( E_{F1} \) : Fermi energy in the bulk (As, Ga)As.
- \( E_{F2} \) : Energy of the second subband in the triangular well.
- \( E_{F3} \) : Difference between the conduction band edge and the Fermi energy in the bulk (As, Ga)As.
- \( n_e \) : Electron density.
- \( \gamma_0 \) : Critical electric field for velocity saturation.
- \( \gamma_1 \) : Critical electric field for velocity saturation.
- \( I_{ds} \) : Drain-to-source current at saturation.

\( k \) : Boltzmann's constant.
\( L \) : Gate length.
\( \mu \) : Low field mobility of the two-dimensional electron gas.
\( N_d \) : Donor concentration in the Al, Ga,As.
\( n_s \) : Sheet carrier density in the two-dimensional electron gas.
\( \phi_b \) : Schottky-barrier height.
\( q \) : Electron charge.
\( Q_T \) : Total charge beneath the gate.
\( R_s \) : Source resistance.
\( R_d \) : Drain resistance.
\( T \) : Temperature.
\( V_F \) : Gate voltage.
\( V_F' \) : Gate voltage minus the threshold voltage.
\( V_{th} \) : Threshold voltage.
\( V_{ds} \) : Drain-to-source voltage at saturation.
\( v_s \) : Electron saturation velocity.

I. INTRODUCTION

MuCh progress has been made in the fabrication of modulation-doped field-effect transistors suitable for high-speed applications [1], [2], [3]. Ring oscillators have operated with a propagation delay of 17.1 ps at 77 K, which is comparable to the performance of Josephson devices [4]. In [5], a simple charge control model was introduced for \( C-V \) characteristics, which is the same as that used for the first order MOSFET modelling. This model assumes that the two-dimensional electron gas is localized in the boundary plane between GaAs and (Al, Ga)As. A piece-wise linear approximation for the electron drift velocity in the two-dimensional layer was used in [5] to calculate the \( I-V \) characteristics.

In the present paper, we describe an improved charge control model which takes into account the dependence of the Fermi level on the gate voltage and the finite width of the two-dimensional gas. (Some preliminary results are given in [6]). We start with the description of the new charge control model. We then calculate \( I-V \) characteristics using a two piece linear approximation for the velocity (as in [5]) and a three piece linear approximation. The latter approximation is necessary to take into account the decrease of the low field mobility with the electric field which is especially important at 77 K for normally-off devices. Finally, we discuss the role of a nonlinear source series resistance and calculate the voltage dependence of the small signal gate-to-source and gate-to-drain capacitances.
II. Charge Control Model

When a doped (Al, Ga)As layer is grown on top of an undoped GaAs layer, a two-dimensional electron gas is formed at the interface due to the difference in the electron affinity of these layers. The amount of charge transfer across the interface is found by equating the charge depleted from the (Al, Ga)As to the charge accumulated in the potential well. A solution is then found such that the Fermi level is constant across the heterointerface. The charge depleted from the (Al, Ga)As is given by [5]

\[ n_d = \sqrt{\frac{2eN_d}{q}} (\Delta E_c - E_F - E_{P1}) + N_{d1}d_1^2 - N_{d1}d_1. \]  

The charge accumulated in the potential well is given by

\[ n_s = \frac{DKT}{q} \ln \left[ \left(1 + e^{\Delta E_F - E_{P1}} \right) \left(1 + e^{-\Delta E_F - E_{P1}} \right) \right] \]  

where \( D \) is the density of states, \( E_0 = \gamma_0 n_0^{2/3} \) and \( E_1 = \gamma_1 n_1^{2/3} \) are the positions of the first two allowed energy levels in the triangular well. The energy reference in the well is the GaAs conduction band edge at the heterointerface. The constants \( \gamma_0 \) and \( \gamma_1 \) and \( D \) are derived in the formalism of the triangular well but have been adjusted slightly to obtain closer agreement with measured subband splitting and electron effective mass \( D = \gamma m^* / \pi \hbar^2 \). Placing a Schottky gate on the (Al, Ga)As results in a certain amount of depletion beneath the gate. If the (Al, Ga)As layer is thick enough or a sufficiently large negative gate voltage is applied, the gate depletion and junction depletion regions will overlap, in which case (1) must be replaced by

\[ n_s = \frac{e}{qd} \left[ V_g - (\phi_b - V_{P1} + E_F - \Delta E_c) \right] \]  

where \( \phi_b \) is the Schottky-barrier height, \( V_g \) is the gate voltage, and \( V_{P1} = qN_{d1}d_1^2/2e \), \( d_1 \) being the thickness of the doped (Al, Ga)As beneath the gate and \( d = d_1 + d_1 \). The simultaneous solution of (2) and (3) then yields the two-dimensional electron gas density \( n_s \) in the potential well for cases with \( n_s \) greater than zero and less than the equilibrium \( n_{eq} \). If the (Al, Ga)As layer is too thick or a sufficiently large positive gate voltage is applied, a parallel conduction path in the (Al, Ga)As is created. For a given \( d_1 \) the maximum gate voltage which affects the two-dimensional electron gas can be obtained by equating (1) and (3) using the Fermi energy at the interface in equilibrium. This condition implies that the (Al, Ga)As underneath the gate is fully depleted.

In the model given in [5] the total charge in the two-dimensional electron gas is found neglecting the variation of the Fermi level with the gate voltage

\[ n_s = \frac{e}{qd} (V_g - V_{off}) \]  

where

\[ V_{off} = \phi_b - \Delta E_c - E_{P1} \]

is the threshold voltage. Using (4) \( I-V \) characteristics of a modulation-doped FET can be found assuming that the current saturation is reached when the electric field at the drain side of the gate is equal to the saturation field \( E_s = \psi_0 / \mu \) [5], [7] where \( \psi_0 \) is the saturation velocity and \( \mu \) is the low field mobility. In a typically normally-off transistor, however, \( E_{F1} \) can be larger than 0.14 V when the device is fully on, causing the charge to be significantly overestimated. The Fermi level \( E_{F1} \) determines the width of the potential well at the interface. As the Fermi level drops, the well becomes wider and the spatial distribution of the electrons changes. As shown below, this effect leads to an increase of about 80 Å in the effective distance from the two-dimensional electron gas to the gate, to a small change in the threshold voltage, to a very pronounced decrease of the transconductance near the threshold and to a "subthreshold" current.

Equation (2) is a quadratic equation with respect to \( qE_{F1}/kT \). The solutions of (2) at 300, 77, and 4 K, respectively, are shown in Fig. 1 (solid lines). The calculated electron density \( n_s \) at 300 K is about half of that predicted by a less accurate three-dimensional electron gas model which neglects the quantization in the potential well and uses the Joyce-Dixon approximation [8]. For the values of \( n_s \) between \( 5 \times 10^{11} \) cm\(^{-2} \) and \( 1.5 \times 10^{12} \) cm\(^{-2} \), these dependencies can be approximated as (shown in dashed lines)

\[ E_{F1} = \Delta E_{F0}(T) + a n_s \]  

where \( a \approx 0.125 \times 10^{-16} \) V \( \cdot \) m\(^{-2} \) and \( \Delta E_{F0} \approx 0 \) at 300 K and \( \Delta E_{F0} \approx 0.025 \) V at 77 K and below. Substituting (5) into (3), we find the modified equation of the charge control model

\[ n_s = \frac{e}{q(d + \Delta d)} (V_g - V_{off}) \]

where

\[ V_{off} = V_{off}^0 + \Delta E_{F0} \]

and

\[ \Delta d = \frac{\Delta \psi}{q} \approx 80 (\text{Å}) \]  

The estimate for \( \Delta d \) given by (8) is in good agreement with the experimental data reported in [8]. The "apparent" mobility for the two-dimensional gas calculated from the drain conductance versus gate voltage curve was 55 000 cm\(^2\) V\(^{-1}\) s\(^{-1} \) at 77 K. The measured mobility was 61 000 cm\(^2\) V\(^{-1}\) s\(^{-1} \). We esti-
mate that the value of $\Delta d$ required to explain this difference is 100 Å, in good agreement with (8). Thus $\Delta d$ gives an important correction especially for a normally-off device where $d$ may be of the order on 300 Å or less.

The implications of this model are shown in Fig. 2. The exact solution of (2) and (3) is shown by the dotted line. This can be compared with the solution of (6) using the linearized $E_{FS}$ versus $n_1$ relation (dashed line) and the charge control model of Delagebeaudoue and Linh where $E_{FS}$ is set equal to zero (solid line). Since $\Delta E_{FS}$ is zero at 300 K, the difference between the two approximations is due to the $\Delta d = 80$-Å increase in the effective gate to two-dimensional electron gas spacing. If we also introduce a threshold voltage $V_{th}$ (see (6)) similar to the threshold voltage of a MOSFET, a substantial "subthreshold" charge exists leading to the subthreshold current. Our modified charge control model, however, is quite adequate for device modeling.

Assuming as in [5], [6] that the current saturation occurs when the electrical field at the drain side of the gate exceeds the velocity saturation field $F_S = V_S / \mu$ and using the Shockley model in order to describe the longitudinal field distribution in the channel below the saturation voltage we find

$$V_{ds} = V' = V_{sat} - (V_{g}^* + V_{s1})^{1/2} + I_{th}(R_s + R_d) \quad (9)$$

and:

$$I_{ds} = \beta V'_{sat} \left[ \sqrt{1 + 2\beta R_s V_{g}^* + V_{g}^* V'_{sat} - (1 + \beta R_s V_{g}^*)^{-1}} \right] \quad (10a)$$

where

$$V_{g}^* = V_{g} - V_{th} \quad (10b)$$

$$V_{sat} = F_L L, \quad \beta = -\frac{q\mu W}{(d + \Delta d) L}.$$  

$V_{ds}$ is the drain-to-source saturation voltage, $I_{ds}$ is the saturation current, $L$ is the gate length, and $W$ is the gate width, respectively.

The normalized drain saturation current for $R_s = 0$ (i.e., $I_{ds} = I_{th} / \beta V_{sat}$) versus normalized gate voltage ($V_S = V'_{sat} / V_{sat}$) is depicted in Fig. 3. Also shown in the drain current from the exact solution of (2) and (3) using the two piece model and the asymptote of (10), i.e.,

$$I_{ds} = \frac{eW}{d + \Delta d} \left[ V_S - V_{sat} \right]. \quad (11)$$

As can be seen in Fig. 3, the agreement is quite good at high gate voltage (above threshold), but there is a considerable subthreshold current flowing as pointed out in [6]. For $V_S$ greater than $V_{sat}$ and $d$ of around 300 Å, our simplified charge control model (6) seems to be quite adequate.

### III. FIELD DEPENDENT MOBILITY

As recent experimental results indicate the mobility of a two-dimensional gas becomes field dependent when the electric field is substantially less than the electric field required to saturate the drift velocity [9], especially at low temperatures. We use a linear three piece approximation of the $u$ versus $E$ curve to take the field dependent of the mobility into account (see Fig. 4).

When the drain-to-source voltage is small the Shockley model applies, leading to

$$I_{DS} = \beta (V'_{g} V_{ds} - \frac{1}{2} V_{ds}^2) \quad (12)$$

for

$$V_{ds} < V_S + V_0 - \sqrt{V'_{g}^2 + V_0^2} \equiv V_{IS}. \quad (13)$$

Here $V_0 = F_L L$. At higher $V_{ds}$

$$V_{IS} < V_{ds} < V_{ds}^*. \quad (14)$$

There are two regions with different differential mobilities under the gate. The first region

![Fig. 2. Surface carrier density versus voltage difference between gate and channel ($V_{g} = 0.15$ V and $d = 400$ Å). Solid line: simple charge control model proposed in [5], [6]. Dotted line: numerical solution from (2) and (3). Dashed line: present model, (6).](image1)

![Fig. 3. Normalized drain saturation current versus normalized gate-to-source voltage ($R_s = 0$). Dotted line: exact solution using two piece model. Solid line: asymptote of (10), (11).](image2)

![Fig. 4. Three piece linear approximation for the velocity field characteristic.](image3)
0 \leq x \leq L_1 \tag{15}

where \( L_1 \) is defined as the point where \( F = F_1 \). In this region the mobility is equal to the low field mobility \( \mu \). In the second region

\[ L_1 < x < L \tag{16} \]

the differential mobility is equal to \( \mu_1 \). In region 1 (see Fig. 4) the current is given by

\[ I_{DS} = C_0 (V'_S - V_1) v_1 \tag{17} \]

where \( v_1 = n(F_1) \) (see Fig. 4).

\[ C_0 = \frac{eW}{q(d + \Delta d)} \quad \text{and} \quad V_1 = V'_S + F_1 L_1 - \sqrt{V'_S^2 + (F_1 L_1)^2}. \]

In region 2 we find

\[ I_{DS} = C_0 (V'_S - V) \left( \mu_1 \frac{dV}{dx} + v_0 \right). \tag{18} \]

Integrating (18) with respect to \( x \) we obtain

\[ L - L_1 = \frac{\mu_1}{v_0} \left[ (V_1 - V_{ds}) + \frac{I_{ds}}{C_0 v_0} \ln \left( \frac{1 - \frac{C_0 v_0}{I_{ds}} (V'_S - V_1)}{1 - \frac{C_0 v_0}{I_{ds}} (V'_S - V)} \right) \right] \tag{19} \]

Equations (17) and (19) are solved numerically to yield \( L_1 \) and \( I_{ds} \).

At the saturation voltage \( V_{ds} = V'_S \), the analytical solution may be found using the following equation

\[ I_{ds} = C_0 (V'_S - V_{ds}) v_1. \tag{20} \]

The result of the solution for (17), (19), and (20) is given by

\[ V_{ds} = V'_S + v_1 \frac{1 - \sqrt{1 + b(V'_S/V_0)^2}}{b} V_0 \tag{21} \]

and

\[ I_{ds} = \frac{b V'_S}{b} \left( \sqrt{b(V'_S/V_0)^2 + 1} - 1 \right) \tag{22} \]

where

\[ b = 1 - 2 \frac{v_1}{v_2} \left( \frac{v_1 - v_0}{v_0} \right) \left( \frac{1 - v_1}{v_1 + v_0} \ln \frac{1 - v_0/v_2}{1 - v_0/v_1} \right) \tag{23} \]

If the source resistance \( R_s \) and the drain resistance \( R_d \) are included, these equations become

\[ I_{ds} = \frac{b V'_S}{b} \sqrt{1 + 2b R_s V'_S/b + (V'_S/V_0)^2} - (1 + b R_s V'_S) \tag{24} \]

and

\[ V_{ds} = V'_S + v_1 \frac{1 - \sqrt{1 + b(V'_S/V_0)^2}}{b} V_0 + I_{ds}(R_s + R_d). \tag{25} \]

The resulting (24) and (25) look quite similar to the simpler equations of the linear two piece model.

IV. SMALL SIGNAL GATE CAPACITANCE MODEL

For simplicity, we calculate the small signal gate capacitance using the two piece model. The total charge \( Q_f \) in the Shockley regime is given

\[ Q_f = W \int_{0}^{L} \frac{dV}{dV} \tag{26} \]

where

\[ C_0 = \frac{-eW}{d + \Delta d}. \]

Then

\[ C_{gs} = \frac{\partial Q_f}{\partial V_g} \tag{27} \]

and

\[ C_{gd} = \frac{\partial Q_f}{\partial V_d} \tag{28} \]

In Figs. 5 and 6, normalized capacitance \( C_{gs}/C_0 \) and \( C_{gd}/C_0 \) are plotted against normalized drain-to-source voltage \( V_{ds}/V_{SS} \) using normalized gate voltage \( V_{gs}/V_{SS} \) as parameter. The calculation is done up to the saturation point. As can be seen from Figs. 5 and 6, over a wide range of voltages each capacitance value is nearly one half of the total gate capacitance. The capacitances are calculated using the charge control model ((14)) and thus our results are not accurate near the threshold voltage.

V. DISCUSSION AND COMPARISON WITH THE EXPERIMENTAL RESULTS

To test the accuracy of the model, a normally-off and a normally-on modulation doped FET fabricated in our lab were selected and characterized. The low field mobility was obtained from the Van der Pauw-Hall measurements of the particular wafer from which the FET was fabricated. The gate width is 145 \( \mu \)m and the length is 1 \( \mu \)m. The heterostructures used to fabricate these FETs were grown by molecular-beam epitaxy on Cr-doped semi-insulating substrates. The structure consisted of consecutively, a 1- \( \mu \)m undoped GaAs buffer layer, a 60-A undoped Al\textsubscript{0.5}Ga\textsubscript{0.5}As layer and a 600-A n-type (Al, Ga)As layer doped with Si to a level of 1 \( \times \) 10\textsuperscript{18} cm\textsuperscript{-3}. The 600-A
dimension was used to allow fabrication of either normally-on or normally-off devices by recessing the gate. For $x = 0.3$, $N_d = 1 \times 10^{18} \text{ cm}^{-3}$, and $d_t = 60 \text{ Å}$, the doped (Al, Ga)As remaining beneath the gate should be about 250 and 350 Å thick to obtain normally-off and normally-on devices, respectively.

The calculated and experimental drain saturation currents at room temperature as a function of the gate voltage are shown in Figs. 7 and 8. $N_d = 1 \times 10^{18} \text{ cm}^{-3}$, $\mu = 0.68 \text{ m}^2 \text{ V}^{-1} \text{ s}^{-1}$, and $R_s = 7 \Omega$ for the normally-on and $10 \Omega$ for the normally-off FET, respectively, are measured. $V_{sat} = 2 \times 10^4 \text{ m/s}$ [9], $F_i = 1 \text{ kV/cm}$ and $F_s = 3.5 \text{ kV/cm}$ are used for our calculation in Figs. 7 and 8 (solid line: three piece velocity model; dotted line: two piece velocity model. The experimental values are marked by the dots). The measured transconductance for the n-on device at 300 K is 225 mS/mm. Even though $10 \Omega$ is measured as $R_s$ for the n-off FET, $12 \Omega$ is used for our model to obtain the best fit to the experimental data. A possible explanation for this is given below. As can be seen from Fig. 7, the agreement between our model and the experimental data is quite good except near the threshold. (This region is not described by the model.) The two piece model overestimates the current predicted by the three piece model by approximately 10–20 percent. The $I_{ds}-V_{ds}$ characteristics for the n-on FET are shown in Fig. 9. As can be seen from the figure, the agreement between the measurement and our calculation is very good.

For the n-off FET, the agreement is also good but the value of $R_s$ has to be adjusted to give a best fit. The slightly smaller current measured at $V_{ds} = 0.8 \text{ V}$ may be due to the fact that our model becomes invalid at gate voltage higher than $V_{off} + (V_{pm})_{2d}$ where

$$V_{p2d} = \frac{q \mu_n d (d + \Delta d)}{\epsilon}$$  \hspace{1cm} (29)

The justification for using $R_s = 12 \Omega$ instead of $10 \Omega$ may be as follows: The fabricated FET has 1-μm spacing between the source and gate. The voltage drop across this region may be so large that $R_s$ should increase as the current increases. This effect should be more pronounced for n-off FET's, even though the surface depletion potential for (Al, Ga)As was reported to be substantially smaller than the Schottky-barrier height [10].

VI. CONCLUSION

A new charge control model for modulation-doped FET's, which takes into account the variation of the Fermi energy of
the two-dimensional electron gas with gate voltage, was developed. This model together with the two and three piece linear approximations for the velocity field characteristic, was used for the analytical calculation of the \( I-V \) characteristics of \( Al_xGa_{1-x}As/GaAs \) FET's in good agreement with experimental results. Small signal gate-to-source and gate-to-drain capacitances are calculated below saturation. Their values are shown to be nearly one half of the total gate capacitance over a wide range of voltages.

REFERENCES


Analysis of Camel Gate FET's (CAMFET's)

ROBERT E. THORNE, SHUN-LIN SU, RUSSELL J. FISCHER, WILLIAM F. KOPP, W. GREGORY LYONS, PAUL A. MILLER, AND HADIS MORKOC, SENIOR MEMBER, IEEE

Abstract—The performance of camel gate GaAs FET's and its dependence on device parameters has been described. In particular, the dependence of the performance on the doping-thickness product of the p⁺ layer was examined. Theoretical calculations indicate that using large p⁺ doping-thickness products provides relatively volatile-independent transconductances and large reverse breakdown voltages, both of which are desirable in large signal applications. Decreasing the p⁺ doping increases the transconductance, which is desirable in logical applications. Comparison of performance of fabricated devices indicates good agreement between theory and experiment over a wide range of structural parameters. Microwave measurements on CAMFET's have yielded a gain of 10 dB at 9 GHz.

1. INTRODUCTION

THE PRINCIPAL type of FET in use at present for high-frequency applications is the MESFET. This device uses a rectifying metal-semiconductor contact for modulating the width of the FET channel. The main virtue of this device is that the submicrometer dimensions required for high-frequency operation are relatively easy to obtain. MESFET's, however, are beset with several problems. The metal-semiconductor contact tends to be unstable, particularly at high operating temperatures, leading to degraded reliability [1]. Further, the barrier height to current conduction is difficult to adjust. Schottky barriers with acceptable characteristics cannot be obtained on some small bandgap semiconductors such as InGaAs unless a tunneling oxide layer is used to enhance the barrier height [2].

An alternative to the MESFET is the JFET, which employs a p-n junction to modulate the channel. The p-n junction gate allows gate biases of up to +1 V to be applied without appreciable gate conduction. However, these devices are relatively difficult to fabricate, particularly with the dimensions required for high-frequency operation. In addition, they require that an ohmic contact be made to a p-type semiconductor, which can lead to large gate resistances. An alternative to the JFET and MESFET has recently been proposed [3]. The camel-gate FET (CAMFET) uses very thin n⁺ and p⁺ layers, which together with the channel form a camel diode [4] to modulate the channel current. Use of the camel