We have proposed the programmable test beds that present the system-level environment to verify and analyze the performance of baseband MODEM schemes and RF/IF hardware for Wideband CDMA (W-CDMA), PCS, CDMA2000, and IMT-2000 systems. These test beds have been implemented with 10 FPGAs for channel CODEC and commercial components for RF/IF transceiver. The DSP boards for real-time H.263 encoding/decoding and hardware channel-emulator have been also used. Therefore, our test beds allow the rapid development of each blocks and enable to reduce Turn-Around-Time (TAT) by easily analyzing the multimedia data communication systems up to 1Mbps/20Mcps. The measurement results show that the performance of our test beds is identical to that of commercial CDMA systems in restrict experimental environments.

2. System Architecture and Characteristics

The proposed test beds have 4 blocks. The first block is H/W channel CODEC, which verifies the performance of various baseband MODEM schemes and signal processors for W-CDMA. The second one is RF/IF transceiver that offers the environment to verify RF/IF hardware components. The third one is source CODEC implemented with DSP boards for real-time H.263 encoding and decoding, which offers the system-level verification environments through multi-media data communication. Finally, hardware channel emulator has been used to emulate the real-time channel environment in the laboratory. Overall system block diagram is described in Fig. 1.

The characteristics of the proposed test beds are as follows: Firstly, it is very easy to verify the performance of the candidate W-CDMA communication schemes, especially IMT-2000 and CDMA2000, because of the programmability of our test beds. Secondly, it is possible to test multi-media data communication up to 1Mbps (of source data rate)/ 20Mcps (of chip rate) in real-time. Finally, it is allowed to support only forward link communication environments for one base-station and one terminal.
3. H/W Channel CODEC

The H/W channel CODEC has channel coding block and channel decoding block. Channel coding block has 4 sub-blocks such as a convolutional encoder, a block interleaver, a walsh code generator and a short PN code generator. Channel decoding block has 6 sub-blocks such as a code acquisition unit, a phase detection unit, a walsh code generator, a short PN code generator, a block deinterleaver and a Viterbi decoder.

Channel CODEC has been implemented with 10 FPGAs (one sub-block in one FPGA).

Channel CODEC is used to verify the performance of various W-CDMA communication schemes, especially IMT-2000 and CDMA2000. The programmable features of each sub-blocks are as follows.

i) Convolutional encoder [1]-[2]
   - Generating polynomial: arbitrary
   - Code rate r: 1/2, 1/3
   - Constraint length k: up to 11
   - Number of ‘0’ padding: It is possible to adjust data transmission speed. It can be set arbitrary.
   - Number of symbol repetition: X 1, X 2, X 4

ii) Block interleaver and deinterleaver [3]
   - Table size: arbitrary

iii) Walsh code generator
   - Code sequence: walsh function
   - Spreading (processing) gain: up to 256 in linear scale.

iv) Short PN code generator [3]
   - Number of states: the number of shift register. It can be set up to 30.
   - Masking polynomial: It is possible to mask the shift register for PN code generation.
   - Generating polynomial: arbitrary
   - Initial state of shift register: arbitrary
   - State period: arbitrary
   - Initial state count offset value: arbitrary

v) Code acquisition [3]-[4]
   - Reference threshold value: arbitrary
   - First integration window size: arbitrary
   - Second integration window size: arbitrary

vi) Viterbi decoder [2]-[3]
   - Trace back depth
   - State metric scaling

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**Figure 2.** Channel coding block diagram
4. RF/IF transceiver

RF/IF transceiver has been implemented with commercial hardware components, of which architecture is similar to the proposed transceiver[5] for IMT-2000 standard.

The modulation scheme is QPSK (Quadrature Phase Shift Keying). The 1st IF is 1855.0MHz and the 2nd IF is 70.0MHz. In the RF transmitter, the input power level can be programmed between -53dBm and +19.5dBm, and the output power level can be also programmed between -49.2dBm and +31.8dBm. In the receiver, the maximum dynamic range is 59dB and the RF input P1dB is -50dBm.

Therefore, our transceiver is so programmable that it can change power level, bandwidth, and the center frequency. Moreover, all the components in the transceiver can be easily replaced by the components that must be verified in the system-level design.

Fig. 4. shows the RF/IF transceiver of the proposed test beds.

5. Performance Analysis

Fig. 5. explains the relation between the processing gain (=Gp), the symbol repetition (=K) and BER. It is well known that Eb/No is proportional to Gp. But, according to our experiments, it is noticeable that Eb/No is proportional to K as well as Gp, because symbol repetition can be interpreted as a symbol repetition code. Hence, in the same chip rate, the transmission power at the lower data-rate (bps) can be reduced against the higher data-rate.
Figure 5. The measured results of the relation between Gp, K, and BER.

Fig. 6 explains the relation between mobile terminal speed and BER. In commercial CDMA systems, fast moving terminals have good BER performance without a closed-loop power control[6]. Our test beds present the same results as shown in Fig.6.

<table>
<thead>
<tr>
<th>Gp K</th>
<th>32kbps</th>
<th>16</th>
<th>1</th>
<th>16</th>
<th>17.2kbps</th>
<th>16</th>
<th>2</th>
<th>32</th>
<th>8kbps</th>
<th>64</th>
<th>1</th>
<th>64</th>
<th>4kbps</th>
<th>64</th>
<th>2</th>
<th>128</th>
<th>1.6kbps</th>
<th>64</th>
<th>4</th>
<th>256</th>
</tr>
</thead>
</table>

\[
\frac{E_b}{N_o \text{ effective}} = \frac{E_c}{N_o} (dB) + 10 \log (G_p \times K)
\]

Figure 6. The measured results of the relation between terminal speed and BER.

Fig. 7 explains the relation between chip rate, multipath fading effects, and BER. Without any rake receiver, all the commercial CDMA systems are seriously affected by the multi-path signals that have the delay longer than a half-chip delay. Notice that our test beds without any rake receivers also tends to be degraded by multi-path fading signals.

6. Conclusion

The new programmable test bed has been implemented to verify and analyze the performance of several baseband MODEM schemes and RF/IF hardware for real-time wireless W-CDMA. Therefore, it allows the rapid development of each blocks and enables to reduce Turn-Around-Time by easily analyzing the multimedia data communication systems up to 1Mbps/20Mcps. The measurement results show that the performance of our test bed is identical to that of commercial CDMA systems in restrict experimental environments.

7. References