

An Integrated Low Power CMOS Baseband Analog Design for Direct Conversion Receiver

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Abstract:

A low power CMOS receiver baseband analog circuit based on alternating filter and gain stage is reported. For the given specifications of the baseband analog block, optimum allocation of the gain, IIP3 and NF of the each block was performed to minimize current consumption. The fully integrated receiver BBA strip is fabricated in 0.18 μm CMOS technology and IIP3 of 30 dBm with a gain of 55 dB and noise figure of 31 dB are obtained at 4.86 mW power consumption.

1. Introduction

Due to the demand of longer battery life and lower cost solutions for wireless personal area network (WPAN) such as IEEE802.15.4, low power single chip CMOS receivers draw great attention [1]. Among the various receiver architectures, the direct conversion receiver (DCR) is a viable candidate solution for low cost and low power.

In a direct conversion receiver as shown in Fig. 1, all in band blockers reach baseband stage without filtering. Thus high linearity performance of baseband analog circuit is required to cope with interferers. Also, those in band interferer limits the allowed gain of the RF front-end and thus the noise performance becomes critical. Since input-referred third-order intercept point (IIP3) and noise figure is approximately proportional to the DC power consumption, it is a great challenge to achieve a compromise of high linearity and low noise performance at low power consumption.

In this paper, optimum allocation of gain, IIP3 and NF of filter stage and gain stage in baseband chain is proposed to minimize current consumption of the overall baseband analog (BBA) chain for a required specification. A receiver BBA circuit is designed and fabricated in 0.18 μm CMOS process. The low power receiver BBA design method is explained in detail and the fabrication results are reported.

2. Design methodology of Baseband Chain to minimize power Consumption

The noise figure and IIP3 performance of the receiver depends on the noise and linearity of blocks as well as their gain. Filtering followed by gain stage suppress out-

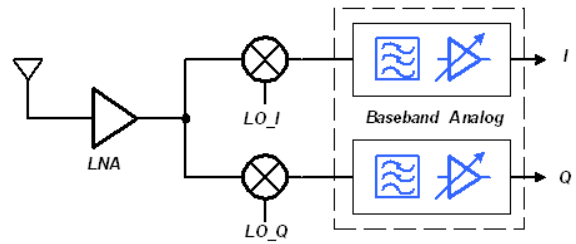


Fig. 1. Baseband analog circuit for direct conversion receiver.

of channel interferers, relaxes linearity requirement of the gain stage. But the low noise channel selection filter is required. Gain stage followed by filtering stage relaxes LPF noise requirements while demanding a high linearity amplifier. At the same power consumption, the structure with the best noise performance leads to the worst linearity performance. Vice versa, a structure with high linearity leads to bad noise performance. To increase noise and linearity performance, more supply current need to be used in the building block. This is not a good way because the current consumption should be minimized. The best way to design the optimum baseband chain is alternating filter and gain stages [2]. This allows better trade-offs between noise figure and linearity for each stage.

To minimize the power consumption for the required specification, the relations between linearity, noise figure and current consumption need to be understood. In this paper, we consider the multi-stage baseband analog chain consists of unit cell with filter and gain function. Cascaded BBA chain model consists of two cells as shown in Fig. 2 can be extended to multi-stage BBA chain.

The theoretical I-V curve of a short channel MOSFET is given as following:

$$I_d = \frac{1}{2} \frac{W}{L} \mu_{\text{eff}} C_{\text{ox}} \frac{V_{\text{GT}}^2}{1 + \theta \cdot V_{\text{GT}}} \quad (1)$$

where $\theta = 1/(E_{\text{sat}} \cdot L)$ and $V_{\text{GT}} = V_{\text{GS}} - V_t$.

Following the analysis in [3], The input referred third-order intercept point (IIP3) of the MOSFET can be obtained as following:

$$V_{\text{IIP3}} \approx \frac{8}{3} \frac{V_{\text{GT}}}{\theta} = KV_{\text{GT}} \quad (2)$$

where $K = 8/(3\theta)$. Using the relation in [4], the IIP3 of Filter and PGA circuit with feedback is given by

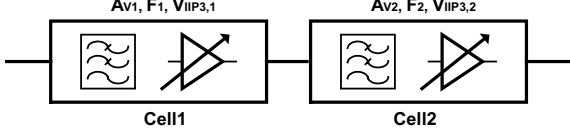


Fig. 2 Baseband analog strip which alternates filters and gain stages.

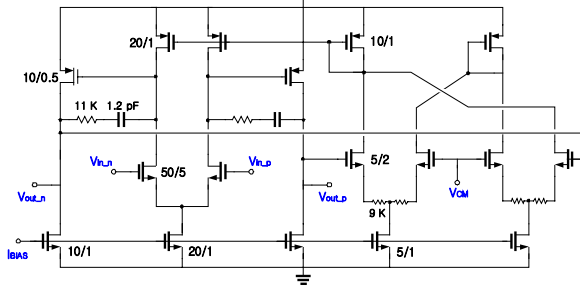


Fig. 3 Two-stage opamp.

$$V_{IIP3}^2 = KV_{GT} \left(1 + \left| \frac{A_o}{A_v} \right| \right)^3 \quad (3)$$

where A_o is open-loop gain and A_v is closed loop gain of two-stage op-amp. We assume that feedback element is linear due to the linear passive element.

In an active-RC filter, both the op-amp and the resistors add noise. The input-referred noise of two-stage op-amp which used in this design as shown in Fig. 3 is determined by the active transistor and the active load of the first stage as following:

$$\frac{V_n^2}{\Delta f} = \frac{8kT\gamma}{g_{mn}} \left(1 + \frac{g_{mp}}{g_{mn}} \right) \quad (4)$$

where $\gamma \geq 3/2$. Then, noise figure of this circuit with respect to the source resistance R_s is

$$F = 1 + \frac{1}{g_m R_s} \left(\gamma + \frac{1}{A_v} \right) \quad (5)$$

The IIP3 and noise figure of each stage is related to the current consumption by spurious free dynamic range (SFDR) as following:

$$SFDR = \left(\frac{IIP3}{F \cdot kTB} \right)^{\frac{2}{3}} \approx \left(\frac{K \cdot I}{kTB(\gamma + 1/A_v)} \right)^{\frac{2}{3}} \cdot \left(1 + \left| \frac{A_o}{A_v} \right| \right)^2 \quad (6)$$

Then, current consumption of each stage is given by

$$I = \frac{1}{2R_s K} \left(\gamma + \frac{1}{A_v} \right) \left(\frac{V_{IIP3}^2}{F} \right) \left(1 + \left| \frac{A_o}{A_v} \right| \right)^{-3} \quad (7)$$

The total current consumption of the baseband chain as shown in Fig. 2 is

$$I_{total} = \sum_{n=1}^2 \frac{1}{2R_s K} \left(\gamma + \frac{1}{A_{v_n}} \right) \left(\frac{V_{IIP3,n}^2}{F_n} \right) \left(1 + \left| \frac{A_o}{A_{v_n}} \right| \right)^{-3} \quad (8)$$

The dynamic range of a cascaded stage is determined by the noise figure, IIP3 and gain of each stage, as following:

$$\begin{aligned} \frac{1}{DR} &= \frac{F}{V_{IIP3}} = \left(F_1 + \frac{F_2 - 1}{A_{v1}} \right) \cdot \left(\frac{1}{V_{IIP3,1}^2} + \frac{A_{v1}^2}{V_{IIP3,2}^2} \right) \\ &= \frac{1}{DR_1} + \frac{1}{DR_2} + \left(\frac{F_1}{V_{IIP3,2}^2} A_{v1}^2 \right) + \left(\frac{F_2 - 1}{V_{IIP3,1}^2} \frac{1}{A_{v1}^2} \right) \end{aligned} \quad (9)$$

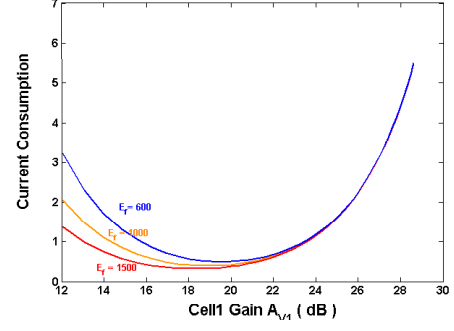


Fig. 4. Current consumption of overall BBA chain versus gain of cell1 (A_{v1})

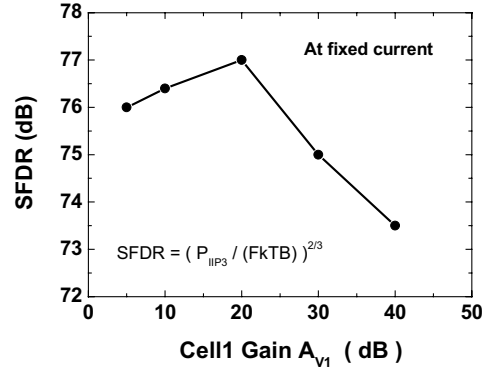


Fig. 5 Transistor level circuit simulation results of spurious free dynamic range (SFDR) versus gain of cell 1 at fixed total current consumption.

Then, the dynamic range of overall cascaded stage is maximized at the following condition:

$$A_{v1}^2 = \sqrt{\frac{F_2 \cdot V_{IIP3,2}^2}{F_1 \cdot V_{IIP3,1}^2}} \quad (10)$$

The third-order intermodulation is unlike an amplifier in that it includes filtering of the input tones. The two-tone interferers are lie in the stop band and attenuated by the filter. So, the IIP3 of the gain stage after filter stage is effectively increased due to the attenuation of interferers by the previous filter bstages. Then, the IIP3 increase factor E_f can be defined as V_{IIP3}^2 (before filtering) $\cdot E_f = V_{IIP3}^2$ (after filtering).

Using the above analysis, (10) can be expressed as

$$\begin{aligned} I_{total} &= \frac{1}{2R_s K} \frac{4V_{IIP3}^2}{F} \left(\gamma + \frac{1}{A_{v1}} \right) \left(1 + \left| \frac{A_o}{A_{v1}} \right| \right)^{-3} \\ &+ \frac{1}{2R_s K} \frac{4V_{IIP3}^2}{F} \frac{1}{E_f} \left(\gamma + \frac{A_{v1}}{A_{total}} \right) \left(1 + \left| \frac{A_{v1} \cdot A}{A_{total}} \right| \right)^{-3} \end{aligned} \quad (11)$$

For a required specification of IIP3, NF and total gain, current consumption is a function of cell1 gain (A_{v1}) and optimum value of A_{v1} can be obtained to minimize current consumption.

Overall current consumption of BBA chain versus cell1 gain is shown in Fig. 4 on condition that maximum gain of BBA chain $A_{total} = 58$ dB and op-amp open loop gain $A_o = 77$ dB. As shown in Fig 4, overall current consumption of BBA chain is affected by choice of cell 1 gain due to the trade-off between noise figure and IIP3.

Table I. Power optimum design parameters at required BBA chain specification.

		Cell1		Cell2	
		LPF1	PGA1	LPF2	PGA2
Sub-block Spec.	Filter order	2nd		4th	
	G (dB)	3	6 ~ 20	3	0 ~ 32
	IIP3 (dBm)	21.5	-3.5	16.5	-27
	NF (dB)	34	31	49	46
BBA chain Spec.	Filter order	6th			
	G (dB)	12 ~ 58			
	IIP3 (dBm)	> 15.5			
	NF (dB)	< 35.7			

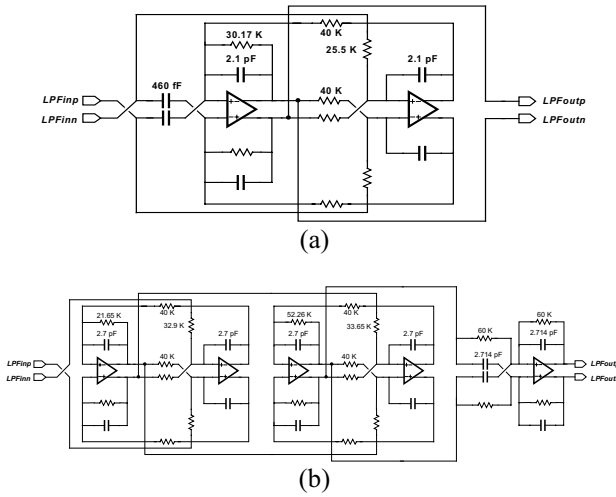


Fig. 6 Schematics of active RC filter (a) LPF1 (b) LPF2.

The current consumption is minimized at the cell 1 gain of 20 dB as shown in Fig. 4. E_f is constant factor depending on the filter order and higher E_f leads to lower current consumption. However, filter order is limited by overall noise figure requirements.

Transistor-level circuit simulation results of SFDR versus cell1 gain at fixed total current consumption are shown in Fig. 5. Maximum SFDR is obtained at the cell1 gain of 20 dB. To Minimize current consumption for a required overall specification leads to same results as maximize overall SFDR for a given current consumption.

A proposed baseband chain is based on Fig. 2, which alternates low pass filter (LPF) stages with programmable gain amplifiers (PGA). With gain step of 35 dB in the RF part, almost 40 dB range of receiver gain programmability needs to be offered by the baseband chain. This results in a PGA range of about from 18 to 53 dB with a resolution of 2dB. Using the proposed optimum design method, optimum allocation of design parameters of each stage for minimum current consumption at required specification of BBA chain is summarized in Table I.

4. Channel Selection Filter

The channel selection filter must provide the required selectivity. An active implementation of the filter must be also low noise so as not to degrade the overall receiver noise figure and be linear enough not to limit the receiver IIP3. The filter power dissipation is a also important

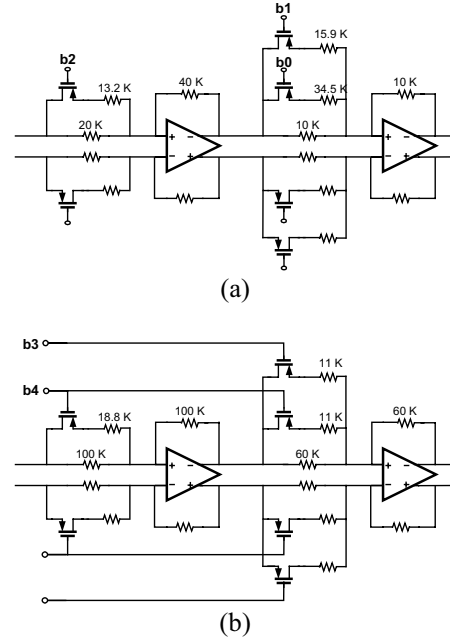


Fig. 7 schematics of programmable gain amplifier (PGA) (a) PGA1 (b) PGA2.

parameter in low power application.

In this design, a second-order Chebyshev low-pass filter (LPF1) and a fourth-order Butterworth low-pass filter (LPF2) have been chosen due to the trade-offs between stopband attenuation and group delay. Additionally, first-order all-pass filter is required for group delay equalization. Active RC filter is very linear due to the linear passive components and high gain op-amps. Active RC filter is suitable for this design due to their high linearity performance compared to the other approach such as G_m -C filter. Active RC implementations of the LPF1 and LPF2 are shown in Fig. 6(a) and Fig. 6(b), respectively.

Each op-amp has to drive a resistive and capacitive load, which requires the use of a two-stage op-amp. Fig. 3 shows the circuit of the two-stage op-amp used in filters and PGA. The first stage transistors are sized properly to minimize the flicker corner frequency. The op-amp has been compensated by using a Miller capacitance of 1.2 pF, along with a 11 k Ω resistor which produces a left-half plane zero and improves the op-amp phase margin. The total current drain of op-amp is equal to 112 μ A. The common-mode level at the op-amp output is set by the CMFB circuit as shown in Fig. 3. One problem of the CMFB circuits is their stability and to reduce the CMFB circuit gain, source degeneration resistors are used.

Each capacitor with an array of digitally controlled switch is used to make the filter tunable. Each unit capacitor in the filter is realized as 5-bit array of capacitances and $\pm 50\%$ tuning range can be achieved, enough to overcome the RC process variations. The tuning accuracy is equal to 3%, which is good enough.

5. Programmable Gain Amplifier (PGA)

As well as in filters, op-amp based amplifiers are used

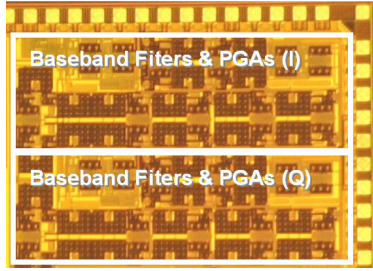


Fig. 8 The chip microphotograph of the baseband analog circuits.

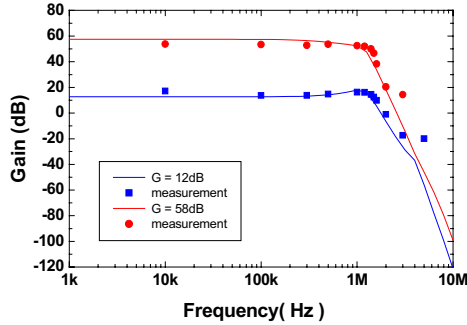


Fig. 9 Frequency response of receiver BBA.

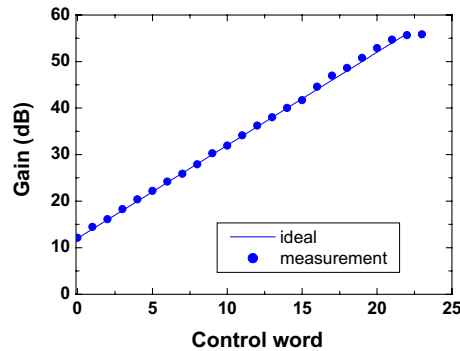


Fig. 10 Programmable gain performance of receiver BBA.

due to excellent linearity performance. Programmable gain amplifiers used in this design are shown in Fig. 7. The different gains are realized by switching the feedback resistors and the resistors in the forward path. All gain stage result in a gain range from 12dB to 58dB with a step of 2dB and gain partitioning of the BBA chain is shown in Table I. The gain of the PGA in decibels changes linearly with control word by digitally controlled 5-bit switch.

With a large maximum gain of about 58 dB at baseband, the output offset of the receiver as well as the input offset of the baseband filter needs to be compensated in some way. A global servo loop is used for DC offset cancellation. DC offset is removed by measuring the output offset and subtracting it at the input using a low pass filter [5]. To keep the constant high pass corner frequency for different gain setting, a programmable gain amplifier in the feedback integrator is used.

5. Experimental Results

The baseband analog circuit (BBA) including filters and PGAs has been fabricated in 0.18 μm 1-poly 6-metal

Table II. Measured performance summary of the receiver BBA.

Noise figure at 50 Ω	31 dB
Gain	12 ~ 55 dB
IIP3 at 50 Ω	30 dBm
Max. Group delay ripple	80 nS
Adj. Ch. Rejection (@5MHz)	72 dB
Current consumption	2.7 mA
Supply voltage	1.8 V
Technology	1P-6M, 0.18 μm

CMOS process. Fig. 8 shows the microphotograph of the BBA. The area of baseband analog circuit including filters, PGA and bias circuit is 1.5 mm^2 .

The frequency response of receiver BBA is shown in Fig. 9. Cut-off frequency is almost same at different gain setting from 12 dB to 55 dB. The simulated frequency response of the receiver is also shown and it is very close to the measured value. The gain characteristics of the receiver BBA with the control words are shown in Fig. 10. The gain of the PGA in decibels changes linearly with control word and error of the gain is smaller than 0.7 dB.

An IIP3 of about 30 dBm at a maximum gain of 55 dB is obtained at 2.7 mA current consumption. In the proposed receiver BBA, high linearity performance is obtained by using active RC filter implementation and high gain op-amp based PGAs. The measurement results of the cascaded receiver BBA are summarized in Table II.

6. Conclusions

A low power CMOS receiver baseband analog circuit based on alternating filter and gain stage is reported. For the given specifications of the baseband analog block, optimum allocation of the gain, IIP3 and NF of the each block was performed to minimize current consumption. The fully integrated receiver BBA strip is fabricated in 0.18 μm CMOS technology and IIP3 of 30 dBm with a gain of 55 dB and noise figure of 31 dB are obtained at 4.86 mW power consumption.

7. Acknowledgement

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8. References

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