Orthogonal Transpose-RAM Cell Array Architecture with Alternate Bit-Line to Bit-Line Contact Scheme

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Abstract
An orthogonal RAM cell array architecture suitable for efficient transposing is proposed, and layout and simulation results are presented. The cell is developed to adopt folded bit-line sensing scheme area-efficiently. The proposed alternate bit-line to bit-line contact scheme in the orthogonal RAM cell array architecture leads to asymmetric bit-line sensing scheme and (i, 2i) bit-line transposing scheme, and results in fast response time of the sense amplifier and low power dissipation for restoring.

1. Introduction

After orthogonal memory was introduced in time-division digital communication [1], it has been used in MPEG2 decoder [2] and soft-output Viterbi algorithm (SOVA) [3] for functionality of serial-to-parallel conversion. In addition, for efficient transposing with one directional internal I/O blocks (or sensing blocks) instead of orthogonal internal I/O blocks, macro of transpose-register was used in 2-D fast Fourier transform (FFT) [4]. However, it consumes much occupied area for size of the 1 bit cell such as 3260μm² (=81.6μm²/1.5μm/1.5μm/4bit, μm: minimum feature size). Even for an extreme case of replacing the transpose-register with a conventional cell of 2Tr-1C, cross-point cell arrangement with bit-line to bit-line contacts (BTBCs) in all bit-lines has several drawbacks if we consider the current scaled DRAM technology and contact scheme for transposing. One is that equivalent bit-line capacitance consists of the vertical bit-line capacitance (Cv) and horizontal bit-line capacitance (Ch) because of the BTBCs in all bit-lines (or diagonal BTBC scheme). As a result, power consumption for restoring cell and response time of the sense amplifier (SA) increase. Another is open bit-line sensing scheme is the only one for cross-point cell arrangements (or open bit-line architecture), which gives rise to small pitch of the SA and high memory array noise. Thus, folded bit-line architecture is preferable in spite of the poor cell area density [5].

As we just mentioned, it is still at issue to solve the drawbacks efficiently. In addition, although dual port memory with the same cell structure of 2 transfer gates is well developed in the literatures [6], orthogonal memory cell architecture is not developed as much as its essential functionality in 2D data processing. Therefore, in this paper, we develop not only new orthogonal transposed-RAM (tRAM) but also its array architecture with folded bit-line sensing scheme and high cell area density. The proposed orthogonal tRAM cell array architecture reduces the equivalent bit-line capacitance by the alternate BTBC scheme.

2. The proposed orthogonal tRAM cell array architecture

2.1 Architecture

The proposed orthogonal tRAM cell array architecture is shown in Fig. 1. If we select a vertical word-line, all horizontal bit-lines are developed by the activated cells, which means open bit-line architecture. While it becomes folded bit-line architecture in terms of the vertical bit-lines since half of them are developed by a horizontal word-line. By using horizontal open bit-line and vertical folded bit-line architecture, we make the number of the vertical bit-lines activated by a horizontal word-line equal to the number of the horizontal bit-lines even if the number of the vertical bit-lines is double. The layout pattern of the 2x2 orthogonal tRAM is shown in Fig. 2, where a pair of poly gates is commonly contacted with metal 1 layer of vertical word-line and finger type-metal 2 layer is used for horizontal bit-line. This layout
scheme makes the minimum feature size of metal 2 layer larger than that of poly such as $8/6\times F_{\text{poly}}$. Thus, cell size is only determined by the $F_{\text{poly}}$ in vertical direction and $F_{\text{m1}}$ in horizontal direction, and the pitch of the SA becomes $4F_{\text{m1}}$ in horizontal direction. Consequently, cell size of the orthogonal tRAM which is composed of 2Tr-1C becomes $16F_{\text{poly}}XF_{\text{m1}}$ in spite of the adoption of the vertical folded bit-line architecture, which is comparable to the cell size of 2Tr-1C with open bit-line architecture [6].

![Diagram](image)

Figure 1: The proposed orthogonal tRAM cell array architecture with alternate BTBCs(a)

2.2 Transposing scheme

For transposing data, we develop an alternate BTBC scheme, where vertical bit-line is alternately contacted with horizontal bit-line as shown in Fig. 1. The alternate BTBC scheme leads to (i, 2i) bit-line transposing scheme that connects the horizontal $i^{th}$ bit-line to the vertical $2i^{th}$ bit-line as well as asymmetric bit-line sensing scheme where one of the pair bit-lines (bit and /bit) has the capacitance of $(C_{\text{vertical}} + C_{\text{horizontal}})$ and the other has the capacitance of $C_{\text{vertical}}$. Therefore, we can nearly cut down restoring power to 75% of the diagonal BTBC scheme.

2.3 Cell operation

The cell operation is as follows. When a cell value is transferred to the bit-line of $C_{\text{vertical}}$ during activation by a horizontal word-line, reference bit-line capacitance becomes $(C_{\text{vertical}} + C_{\text{horizontal}})$ and vice versa. While, the capacitances of the signal and reference bit-line are always $(C_{\text{vertical}} + C_{\text{horizontal}})$ and $C_{\text{vertical}}$, respectively, in the case of the activation by a vertical word-line. Their activated values are sensed by the SAs that are connected to the vertical bit-lines to utilize the folded bit-line sensing scheme. Considering the conventional cross-coupled CMOS SA in Fig. 1, the open loop gain $T$ of the SA for orthogonal tRAM cell array with the alternate BTBC scheme is found to be (1). Therefore, it shows higher performance than the diagonal BTBC scheme where $sRdxC_{\text{vertical}}$ becomes $sRdx(C_{\text{vertical}} + C_{\text{horizontal}})$.

$$T(\text{alternate BTBC}) = \frac{g_m \times R_d}{1 + sR_d \times (C_{\text{horizontal}} + C_{\text{vertical}})} \times \frac{g_m \times R_d}{1 + sR_d \times C_{\text{vertical}}}$$

(1)

In (1), the transconductances of the p-channel and n-channel devices have been lumped into a single equivalent $g_m$ and $R_d$ includes the parallel combination of the output resistance of both n- and p-channel devices of conventional cross-coupled CMOS SAs in Fig. 1.

![Diagram](image)

Figure 2: The layout of the 2x2 orthogonal tRAM cells (Alternate BTBC is not shown)
3. Spice Simulation Result

We simulate reading and restoring operation of the proposed orthogonal tRAM cell array architecture with the conventional cross-coupled CMOS SAs in Fig. 1. The results are shown in Fig. 3, where the cells of '00' and '10' are involved and all logic states of the cells are initially assumed to be '1'. The simulated results of the diagonal BTBC scheme are also shown for comparison. From the enable signal of the SA (SA:On), the response time takes 2.75ns for the alternate BTBC scheme and 3.25ns for the diagonal BTBC scheme to reach 3.0V difference in bit-lines. This shows faster operation of the proposed cell array architecture. The reading of '10' cell by a vertical word-line such as a V_WL0 is also shown for illustration of (1, 2) bit-line transposing scheme. In the case of reading by V_WL0, its value is transferred to the bit-line of V_BL2 and sensed in SA:B instead of the V_BL1 and SA:A during reading by H_WL1. In Table I, the features of the orthogonal tRAM cell are summarized.

<table>
<thead>
<tr>
<th>Table I. The features of the orthogonal tRAM cell</th>
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<tr>
<td>Cell (2Tr-1C) Size</td>
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<td>Contact scheme</td>
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<td>Bit-line capacitance</td>
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4. Conclusion

In this Paper, we have developed an orthogonal tRAM cell array architecture suitable for transposing that frequently happens in 2-D data processing and presented the layout pattern of the orthogonal tRAM and simulation results. The cell size occupies 16F_{poly}×F_{mil} with folded bit-line sensing scheme. By the alternate BTBC scheme, we achieve (1, 2) bit-line transposing scheme and reduce the response time of the SA and power dissipation for restoring. Therefore, it is found to be a promising cell array architecture for orthogonal memory arrangements.

References


Figure 3: The spice simulated waveforms of the orthogonal tRAM cell array (solid line: alternate BTBC scheme, dashed line: diagonal BTBC scheme)