Effect of p-i-p⁺ Buffer on Characteristics of 
n-Channel Heterostructure 
Field-Effect Transistors

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Abstract—In order to reduce the two major problems of short-channel effects and limited threshold voltage controllability in submicrometer gate heterostructure FET's (HFET's), a p-i-p⁺ structure in the buffer is investigated. The p layer is adjacent to the channel and the p⁺ layer is located fairly far from the channel. This structure lowers the electrostatic potential in the buffer under the channel, which reduces the current in this region. Monte Carlo simulation shows that such a buffer decreases the output conductance in saturation by 80% for a 0.3 μm gate-drain Modulation Doped FET (MODFET) with n⁺ self-aligned source and drain regions. The p⁺ layer has the additional purpose of enabling adjustment of the threshold voltage by way of changing the potential of the p⁺ layer externally. Our one-dimensional calculations for the modulation-doped AlGaAs/GaAs heterostructures show that a 0.1-V variation of the threshold voltage can be adjusted by a 2-V variation of the back bias when the p⁺ layer is located 5000 Å away from the channel. However, the maximum carrier density in the 2-D gas becomes quite limited when high negative bias is applied to the p⁺ layer or when the distance from the p⁺ layer to the heterointerface is decreased. This limitation is less severe in doped structures where n_max is approximately 70% larger. In Doped Channel HFET (DCHFET) structures, the p⁺ layer can be brought very close to the n⁺ doped channel without any important restrictions on n_max in the channel. The p layer sheet doping density must also be restricted to approximately 1.5×10¹² cm⁻² for the MODFET in order to avoid a large reduction of n_max. Again, this limitation is not important in DCHFET devices. Therefore, use of the p-i-p⁺ buffer is more advantageous for doped MODFET's than for uniformly doped MODFET's, and even more so for DCHFET's, where larger charges in the p-i-p⁺ buffer are required to limit the short channel effects.

Nomenclature

d_h Doped GaAs channel layer thickness (m).
d_i Undoped GaAs layer thickness from the heterointerface to the p layer (m).
d_p Doped GaAs layer thickness (m).
d_p⁺ Doped GaAs layer thickness from the p layer to the p⁺ layer (m).
\Delta W Effective width of the 2-D gas (m).
E_q Difference between the Fermi level and the bottom of the conduction band in thermal equilibrium for the doped GaAs channel layer (eV).
E_g In subband energy level in the 2-D gas (eV).
E_f GaAs bandgap energy (eV).
F_eff Effective electrical field at the heterointerface in GaAs (V/m).
F_per Electrical field at the heterointerface in GaAs (V/m).
\hbar Planck's constant (J·s).
\kappa Boltzmann's constant (J/K).
m_e Effective electron mass of GaAs (kg).
N_d Dop ing density in the p layer (m⁻³).
N_d⁺ Doping density in the doped AlGaAs layer (m⁻³).
N_d⁺⁺ Dop ing density in the doped GaAs channel layer (m⁻³).
N_d⁺⁺⁺ Doping density in the uniformly doped MODFET's, where larger charges in the p-i-p⁺ buffer are required to limit the short channel effects.
\n_s Sheet electron doping density in the AlGaAs layer (m⁻³).
\n_s Max imum sheet electron density in the channel (m⁻²).
\n_s Electron charge (C).
\n_s Charge in the gate metal (C/m²).
T Temperature (K).
V_G Gate voltage (V).
V_{sub} Bottom of the conduction band in the GaAs at the heterointerface measured from the Fermi level (eV).
V_{th} Substrate bias (V).
V_{th} Threshold voltage (V).
\Delta \chi Depletion width at the heterointerface in the doped GaAs channel layer (m).
\Delta \chi Depletion width at the channel/buffer interface in the doped GaAs channel layer (m).
\Delta \chi Conduction band discontinuity at the heterointerface (eV).
\varepsilon_{r} Permittivity of AlGaAs (F/m).

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E_2 \quad \text{Permittivity of GaAs (F/m)}.
\phi_b \quad \text{Schottky-barrier height (V)}.

I. INTRODUCTION

OVERTHE past several years, n-channel heterostructure field-effect transistor (HFET) integrated circuits have demonstrated impressive performance [1]. However, the limited threshold-voltage controllability, especially from wafer to wafer, still makes large-scale commercial production difficult. Another problem is a relatively low gate turn-on voltage (0.8-1.0 V), compared to silicon technology. In addition, the gate length has recently decreased to about half a micron, which makes the controllability more difficult because of short-channel effects. Recently, an HFET with a p⁺ gate (a \pi-HFET) and a p-i-p⁺ buffer layer was proposed in order to overcome these difficulties [2]. The p layer is adjacent to the channel. It is depleted and thus does not contribute to the parasitic capacitance. The p⁺ layer is located fairly far away from the channel in order to avoid an increase in the parasitic capacitance. This structure lowers the electrostatic potential in the buffer under the channel, thereby reducing the short-channel effects. P-type doping in the buffer layer has been demonstrated to have such an effect in GaAs MESFET technology [3] and in Si n-MOS technology [4]. The p⁺ layer has the additional purpose of enabling adjustment of the threshold voltage by way of changing the potential of the p⁺ layer externally. This back-bias effect was examined by Schueremeier et al. in order to study the confinement of the two-dimensional electron gas at the heterointerface [5]. The p⁺ layer can be accessed through vias, which can possibly be common to all devices on a chip. (See [2] for a more comprehensive discussion of this issue.) In this paper, we will present the carrier concentration in HFET's with the p-i-p⁺ buffer as a function of the gate bias, obtained by self-consistent one-dimensional calculation of 2D electron density, subband levels, and electrostatic potential. These results will quantify certain limitations on the ranges of geometrical and doping parameters and allow us to optimize the HFET design and to compare Modulation Doped FET (MODFET) and Doped Channel HFET (DCHFET) structures. Furthermore, Monte Carlo simulations demonstrate that this p-i-p⁺ buffer drastically reduces the short-channel effects.

II. RESULTS AND DISCUSSION

A. Uniformly Doped MODFET

The schematic band diagram under the gate of the p-i-p⁺ buffer AlGaAs/GaAs structure is shown in Fig. 1. Here, the AlGaAs layer is uniformly doped. In order to solve the Poisson equation for the region, we use the following assumptions:

a) All dopants except those in the p⁺ layer are ionized and the depletion approximation is valid.
b) Free electron charge at the heterointerface only is considered, and the thickness of this 2-D electron gas is neglected.

c) The Fermi level is constant throughout the AlGaAs and GaAs regions.

Using these assumptions and solving the Poisson equation from the gate metal to the AlGaAs side of the 2-D gas interface and from the GaAs side of the 2-D interface to the p⁺ layer, respectively, the following equations are obtained:

\[ V_s = \phi_b - \Delta E_r + V_0 - \frac{qN_e d_2^2}{2e_1} + \frac{\epsilon_2}{\epsilon_1} F_s (d_n + d_i) \]  \hspace{1cm} (1)

\[ E_s = V_{sub} + V_0 \]

\[ = F_s (d_1 + d_2 + d_3) - \frac{qN_e (d_1 + d_2 + d_3)}{\epsilon_2} \]

\[ + \frac{qN_e d_2 \left( \frac{d_3}{2} + d_3 \right)}{\epsilon_2} \]  \hspace{1cm} (2)

The relation between the subband energy levels and the electrical field in the quantum well is given by

\[ E_i = \left( \frac{\hbar^2}{8m^* \pi^2} \right)^{1/3} \left[ \frac{3qF_{eff} \pi}{2 \left( \frac{3}{4} \right)^{2/3}} \right] \]  \hspace{1cm} (3)

Here we use the triangular potential well approximation and the effective electrical field \( F_{eff} \) [6], which is the average of the electrical fields at the heterointerface and that in the undoped buffer adjacent to the 2-D gas. From Gauss' law, that field in the buffer is expressed by

\[ F_s = \frac{qn_s}{\epsilon_2} \]

Therefore, the effective field is given by

\[ F_{eff} = F_s = \frac{qn_s}{2\epsilon_2} \]  \hspace{1cm} (4)

This effective electric field approach was originally suggested by Stern and Das Sarma [7] and has been proven to give a very good correspondence with exact quantum-mechanical calculations [6]-[9]. The 2-D gas concentration \( n_s \) is related to the differences between the subband energy levels \( E_i \) and the level of the conduction band in the GaAs at the heterointerface \( V_0 \) [10]

\[ n_s = \sum_{i=0}^{n_0} \frac{4\pi m^* kT}{\hbar^2} \ln \left[ 1 + \exp \left( \frac{q(V_0 - E_i)}{kT} \right) \right] \]  \hspace{1cm} (5)
We include only the two lowest subbands in the calculation because we do not consider the subthreshold region. By solving (1)-(5) self-consistently, we can find the relation between the applied gate voltage and \( n_s \) for different values of the buffer layer parameters. If (2) and (4) are substituted by

\[
q n_s = \varepsilon_2 F_s \quad (2a)
\]

and

\[
F_{\text{eff}} = F_s \quad (4a)
\]

respectively, we recover the characteristics of the conventional MODFET without the p-i-p' buffer.

At larger positive gate voltages, \( n_s \) saturates at a certain maximum value \( n_s \text{max} \), since the doped AlGaAs layer becomes partially undepleted. Here we assume that such a saturation occurs when the minimum of the conduction band level in the doped AlGaAs layer has the same separation from the quasi-Fermi level as that of bulk AlGaAs with the corresponding doping density in thermal equilibrium.

The calculations are performed for devices with a 200 Å-thick doped AlGaAs layer of doping density \( N_d = 3 \times 10^{18} \text{ cm}^{-3} \), and a 30-Å-thick spacer AlGaAs layer (unless specified differently below).

Fig. 2 shows the dependence of \( n_s \) on the applied gate voltage at varying substrate p'-layer bias. As can be seen from the figure, the threshold voltage is controlled by the substrate bias. For example, a 2-V change in substrate bias causes a 0.1-V threshold voltage change in this structure. This controllability significantly reduces the process requirement for the threshold voltage. However, note that whereas positive back bias, up to approximately 1.0 V, can cause an increase in \( n_s \text{max} \), negative back bias causes a reduction. In addition, reducing the distance from the interface to the p' layer also acts to reduce \( n_s \text{max} \), as seen in Fig. 3. Comparison with the dashed curve, representing the conventionally designed MODFET, reveals that a large distance from the p' layer to the p-layer, approximately 500 Å, is required to retain a saturation value comparable to that of the conventional structure. It is interesting to note that even when the doping density in the doped AlGaAs layer is increased for the structure with the small \( d_s \) value of 500 Å, \( n_s \text{max} \) remains small (see Fig. 4). In this respect, a conventional MODFET structure markedly differs from DCHFET's as discussed later.

The increase in the gate capacitance \( C_g \) with the decrease in \( d_s \) at gate voltages below the threshold voltage is another disadvantage associated with small \( d_s \) values (see Fig. 5). The capacitance \( C_g \) is calculated by differentiating the total charge on the gate metal \( Q_m \) with respect to the applied gate voltage. The gate charge is calculated using the following equation:

\[
Q_m = qN_d d_s - \varepsilon_2 F_s \quad (6)
\]

Fig. 6 identifies another parameter limitation of the p-i-p' buffer. This figure shows the dependence of \( n_s \) on the p-layer doping density at a p-layer thickness of 300
Fig. 5. $C_g-V_g$ characteristics for different distances from the p layer to the p$^+$ layer $d_l$. ($d_l = 300 \text{ Å}, d_2 = 300 \text{ Å}, N_n = 5 \times 10^{16} \text{ cm}^{-2}, V_{sub} = 0 \text{ V}$)

Fig. 6. $n-V_g$ characteristics for different doping densities in the p layer $N_n$. ($d_l = 300 \text{ Å}, d_2 = 300 \text{ Å}, d_3 = 4400 \text{ Å}, V_{sub} = 0 \text{ V}$)

Fig. 7. $n-V_g$ characteristics for different distances from the p layer to the p$^+$ layer $d_l$ using the simple set of equations. ($d_l = 300 \text{ Å}, d_2 = 300 \text{ Å}, d_3 = 4400 \text{ Å}, N_n = 5 \times 10^{16} \text{ cm}^{-2}, V_{sub} = 0 \text{ V}$)

\[ \Delta d = \frac{\epsilon_0 E_0}{q n_{max}}. \]  

The first term on the right-hand side of (7) represents the relation between $n_t$ and the gate voltage in the case of zero buffer doping. The second term can be interpreted as the total charge due to the inserted p layer and the third term is the charge in the p$^+$ layer. For simplicity, the $V_0$ term in the third term on the right-hand side of (7) is neglected since this value is relatively small. $n_{max}$ is obtained by using the value of the equilibrium 2-D charge carrier density in the AlGaAs/GaAs heterostructure system [11] (without the effects of gate electrode and buffer doping), instead of using the first term in (7). The results are shown in Fig. 7. Here, 60 Å is used for $\Delta d$, which is determined from the self-consistent calculations using (1)-(5). These results are found to agree fairly well with those obtained by the more accurate equations (compare with Fig. 3). However, the accurate calculation indicates that $\Delta d$ and the total charges in the buffer and the heterointerface channel are slightly dependent on the p- and p$^+$-layer parameters, which is not considered in this simple calculation.

### B. δ-Doped MODFET

In the case of δ-doped MODFET's, (1) has to be modified as follows:

\[ V_g = \phi_b - \Delta E_c - V_0 - \frac{qN_{qd}d_0}{\epsilon_1} + \frac{\epsilon_2}{\epsilon_1} F_s(d_n + d_l). \]

Here $N_{qd}$ is the sheet carrier density in the AlGaAs layer. $n_{max}$ is obtained when the lowest eigenstate energy in the δ-doped AlGaAs layer coincides with the Fermi level [12]. Fig. 8 shows the characteristics, using the same parameters as used for the MODFET structures in Fig. 3, $N_q = 0$, and $N_{qd} = 3 \times 10^{12} \text{ cm}^{-2}$. As can be seen, this structure has a higher $n_{max}$, approximately 70%, which makes the negative effects of the p-i-p$^+$ buffer less severe.
Using the optimized p-i-p⁺ structure from the above considerations, we compared a 0.3-μm gate length δ-doped self-aligned MODFET with such a buffer to the same device with a conventional buffer, employing a self-consistent ensemble Monte Carlo simulator. The electrons in these simulations are treated within a classical bulk formalism, employing bulk band structure as well as bulk scattering rates. Such an approach is chosen to reduce computational times, and is not believed to influence our results much, since in high-field regimes the two-dimensional properties of the channel are not very prominent [13]. Poisson's equation is solved by the finite difference solver POT4A [14]. A more detailed description of the simulator is given elsewhere [15].

The cross section of the simulated FET with p-i-p⁺ buffer is shown in Fig. 9. The doping density in the n⁺ regions is $1 \times 10^{18} \text{ cm}^{-3}$ and the contact region depth, taken from the heterointerface, is 750 Å in this simulation. For the MODFET with p-i-p⁺ buffer, $d_1 = 300$ Å, $d_2 = 600$ Å, $d_3 = 3000$ Å, and the doping density $N_a = 2.5 \times 10^{16} \text{ cm}^{-3}$ in the p layer are used. The lower boundary of the simulated device is taken at the bottom of the i layer. The potential at this boundary is fixed to the value corresponding to the back bias, thus representing the p⁺ layer. For the conventional MODFET, the potential at the lower boundary is floating.

Comparison of the output conductance $g_d$ in the saturation region in the two structures reveals that $g_d$ is reduced by about 80% (from approximately 50 to about 10 mS/mm). Fig. 10 shows the electrostatic potential as a function of perpendicular position $y$ at a lateral position 0.08 μm into the channel from the source contact region. As can be seen, in the case of the p-i-p⁺ structure, the potential in the buffer is reduced and a high transverse electrical field of about 20 kV/cm is present. This electrical field significantly enhances electron confinement to the channel, thereby reducing the electron density in the buffer, as shown in Fig. 11. Thus the buffer current is deal a major blow. The connection between short-channel effects and charge injected from the source contact into the buffer as well as the dependence of short-channel effects on gate length and contact depth were established in [15]. There, it was shown that such charge injection is the dominant source of short-channel effects in self-aligned HFET's in this gate-length range. Thus an adequate confinement in the first part of the channel is essential. At longer gate lengths, other effects such as gate length modulation and real space transfer into the buffer close to the drain contact become increasingly important.

In these simulations, no attempt has been made to distinguish the effects of the p layer from those of the p⁺ layer. However, from simple one-dimensional calculations we estimate that the p layer reduces the potential 30 Å beneath the heterointerface by about 20 to 30 meV at this p layer doping density, whereas the contribution from the p⁺ layer at the same position is roughly 100 meV. Thus the p⁺ layer is the dominant contributor to the confinement, although the effect of the p layer is far from insignificant. From a fabrication point of view, it may be argued that under such conditions the p layer may be removed in order to avoid a degradation of channel velocities from diffusing dopants.
C. DCHFET

The following equations describe the doped channel HFET’s shown in Fig. 12,

\[ V_s = \phi_n - \Delta E_e + E_{ch} - \frac{qN_{ch}d_{det}}{\epsilon_1} \left( d_i + \frac{d_{det}}{2} \right) \]  \hspace{1cm} (11)

\[ E_{th} = V_{sub} + E_{ch} = \frac{qN_{ch}d_{det}}{\epsilon_2} \left( \frac{d_{det}}{2} + d_1 + d_2 + d_3 \right) \]

\[ qN_{ch}d_z \left( \frac{d_z}{2} + d_3 \right) \]

\[ n_1 = N_{ch}(d_{ch} - d_{det} - d_{det}). \] \hspace{1cm} (13)

We assume that the maximum value of \( n_1(n_{nax} = n_{nax}) \) is reached when the depletion width in the doped GaAs channel layer at the AlGaAs/GaAs heterointerface \( d_{det} \) is equal to zero. This is a low bound estimate because the device can actually operate in the enhancement mode. The calculations are performed using the same same total AlGaAs thickness as in the MODFET case, i.e., 230 Å. Fig. 13 shows that the DCHFET threshold voltage can be also controlled quite well by the substrate bias. In addition, the DCHFET has the significant advantage of a much higher \( n_{nax} \) compared with MODFET’s. Even when the \( p^+ \) layer is located close to the channel, the values of \( n_{nax} \) remain high (compare with Fig. 4) and can be further increased by using higher densities (as shown in Fig. 14) and/or thicker channels.

III. CONCLUSION

A p-i-p\(^+\) buffer structure was optimized by considering the channel carrier density \( n_i \) obtained by one-dimen-
sional calculations. The results clearly show that the threshold voltage for both MODFET's and DCHFET's can be controlled well by the application of bias to the p⁺ layer. The results also point out that the distance from the p⁺ layer to the channel in MODFET structures must be relatively large since the maximum carrier concentration \( n_{\text{max}} \) in the 2-D gas decreases when reducing this distance. The p-layer sheet concentration in MODFET's must also be restricted to approximately \( 1.5 \times 10^{11} \text{cm}^{-2} \) in order to avoid a large reduction of \( n_{\text{max}} \). This limitation is somewhat less severe in the 6-doped structures where \( n_{\text{max}} \) is approximately 70% larger. Monte Carlo simulation shows that this optimized p-i-p⁺ structure reduces the output conductance by approximately 80% for a self-aligned 0.3-μm gate 6-doped MODFET. In DCHFET's, the problem of large \( n_{\text{max}} \) reduction can be avoided because the channel charge is not limited by the accumulation of charge in a charge-control layer. Hence, we conclude that the p-i-p⁺ buffer has more advantages when used in 6-doped MODFETs than in uniformly doped MODFET's, and even more so for DCHFET's. This advantage is more important for shorter gate lengths or deeper p⁺ regions because of the pronounced short-channel effects. The p-i-p⁺ buffer concept may also be applied to other devices than those studied here.

**REFERENCES**


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