Source, Drain, and Gate Series Resistances and Electron Saturation Velocity in Ion-Implanted GaAs FET's


Abstract—Techniques which allow us to determine the source, drain, and gate resistances and the electron saturation velocity of ion-implanted GaAs FET's are described. These techniques are based on the "end" resistance measurements. The theory of this method is developed and used for a new interpretation of the "end" resistance measurements. The values of the series resistances determined by this technique are shown to be in an excellent agreement with those obtained by the modified Fukui method. The values of the electron saturation velocity varying from 1.0 x 10^7 m/s to 1.3 x 10^8 m/s are obtained using the end resistance method. The proposed set of measurements is simple and accurate enough to be used as a routine characterization technique for GaAs FET's.

I. INTRODUCTION

The source and drain series resistances \( R_s \) and \( R_d \) are key parameters which determine the performance of field-effect transistors. The source series resistance strongly affects the device transconductance and noise figure. Both series resistances increase the power consumption and slow down the device operation. An accurate measurement of the series resistances is crucial for the reliable determination of the effective electron saturation velocity in the channel of a short-gate field-effect transistor. The values of the series resistances are also required for the device and circuit modeling.

Series resistances may vary from device to device because of changes in the contact resistance which is difficult to calculate theoretically. This makes an experimental determination of series resistances even more important.

Hower and Bechtel [1] obtained the sum of the source \( R_s \) and drain \( R_d \) resistances by measuring the small-signal drain-source resistance \( r_{ds} \) at zero drain-source voltage as a function of the gate voltage

\[
r_{ds} = R_s + R_d + \frac{1}{G_0 (1 - \sqrt{\eta})}
\]

where \( G_0 = q\mu a N / L \) is the full channel conductance, \( \eta = (V_{BI} - V_{gs})/V_{po} \), \( a \) is the active channel thickness, \( \mu \) is the mobility, \( N \) is the doping density, \( W \) is the channel width, \( L \) is the channel length, \( V_{po} \) is the pinchoff voltage, \( V_{BI} \) is the built-in voltage, and \( V_{gs} \) is the gate-source voltage. The measured values of \( r_{ds} \) were plotted as a function of \( 1/\sqrt{\eta} \). The value of \( V_{po} \) was adjusted to yield a good linear fit. The values of \( R_s + R_d \) were determined from the intercept. This method, however, may not be accurate enough for ion-implanted GaAs FET's because it does not take into account the nonuniform doping and mobility profiles. In [2] this method was extended to include the nonuniform doping and mobility profiles, based on the iterative solution using the depletion approximation. This approach, however, only allows us to determine the sum of \( R_s \) and \( R_d \), not their values separately.

Fukui [3] suggested to determine the difference between \( R_d \) and \( R_s \) from the measurements of the gate-source and gate-drain current-voltage characteristics. This approach was combined with the iterative technique [2] to determine \( R_s \) and \( R_d \). Recently, it was proposed to use the "end" resistance measurements [4], [5] in order to determine \( R_s \) and \( R_d \) [6] - [8] and the electron saturation velocity \( v_d \) [9]. As we show in this paper, our results do not agree with the results of [6], but they are in agreement with the results obtained in [7], [8]. At large gate currents, however, the velocity saturation effects have to be included in order to explain the experimental results. Moreover, we show that using the same technique we are able to determine quite accurately the gate series resistance in addition to the source and drain series resistances.

II. "END" RESISTANCE MEASUREMENT TECHNIQUE

The basic idea of the "end" resistance measurement technique is illustrated by Fig. 1. In this scheme the flowing gate current creates a voltage drop across the series resistance \( R_s \) and the drain contact is floating so that the drain section of the device acts as a "probe." Hence, the source series resistance has been estimated as...
is the gate potential, \( V_g \) is the gate voltage, \( R_s \) is the gate series resistance, \( V_I' \) is the potential at the source side of the channel under the gate, \( V_D' \) is the potential of the drain side of the channel under the gate, and \( V_{po} \) is the pinchoff voltage. In a typical experimental situation

\[
V_d - V_s << V_{BI} - V_g
\]

and (6) is fulfilled.

The gate current density \( J_g(x) \) is given by

\[
J_g(x) = J_s \exp \left[ \frac{V_g' - V}{nV_T} \right]
\]

(8)

where

\[
J_s = A_s T^2 \cdot \exp \left[ \frac{qV_{BI}}{kT} \right]
\]

(9)

is the gate saturation current, \( A_s \) is the effective Richardson constant, \( T \) is temperature, \( n \) is the ideality factor, \( V_T = kT/q \) is the thermal voltage. As the gate current density is the exponential function of \( V \) whereas \( r_{ch} \) is relatively weak function of \( V \) (see (6) and the related discussion), we can take into account the nonuniform distribution of the gate current under the gate assuming at the same time that \( r_{ch} \) is nearly independent of \( x \). In (8) we neglected by the reverse gate current and hence it is valid only for \( V_g' - V >> nV_T \).

The boundary conditions are

\[
dV \over dx = -J_g r_{ch} \cdot W \quad \text{at} \quad x = 0
\]

(10)

and

\[
dV \over dx = 0 \quad \text{at} \quad x = L
\]

(11)

(see Fig. 1).

Differentiating (5) with respect to \( x \) we find

\[
d^2V \over dx^2 = -J_g r_{ch} \cdot \exp \left[ \frac{V_g' - V}{nV_T} \right]
\]

(12)

or, using (4)

\[
\frac{d^2V}{dx^2} = \frac{r_{ch}}{W} \cdot J_g \cdot \exp \left[ \frac{V_g' - V}{nV_T} \right]
\]

(13)

The integration of (13) with boundary conditions (10) and (11) yields

\[
I_g' = \frac{2J_g \cdot W \cdot nV_T}{r_{ch}} \exp \left( \frac{V_g'}{nV_T} \right) \left[ 1 - \exp \left( \frac{V_{ds}'}{nV_T} \right) \right]
\]

(14)

and

\[
L = \left[ \frac{2nV_T}{J_g r_{ch}} \right]^{1/2} \cdot \exp \left[ \frac{1}{2nV_T} (V_{ds}' - V_{gs}') \right] \cdot \tan^{-1} \left[ \frac{\exp \left( \frac{V_{ds}'}{nV_T} \right) - 1}{1/2} \right]
\]

(15)

Equation (15), which may be rewritten as
\[ I_d = 2^{1/2} \exp \left( \frac{u_d - V}{2} \right) \tan^{-1} \left[ \exp \left( u_d + 1 \right) \right]^{1/2} \]  
has to be solved together with (14), which may be rewritten as

\[ i = 2 \cdot \exp \left( \frac{u_d}{2} \right) \left[ 1 - \exp \left( -u_d \right) \right]^{1/2} \tan^{-1} \left[ \exp \left( u_d + 1 \right) \right]^{1/2}. \]  

Here

\[ l_0 = \frac{L}{J_{ch}^2 V_T^{-1}} \]

\[ i = I_g \cdot \frac{R_{ch}}{n V_T} \]

\[ v_d = \frac{V_{ds}}{n V_T} \]

\[ y = V_{gs}/n V_T. \]

At small values of \( v_d \ll 1 \), (17) may be simplified.

\[ i \approx 2v_d \left[ 1 + \frac{v_d}{6} \right] \]  

(18)

or

\[ v_d \approx \frac{i}{2} \left( 1 - \frac{i}{12} \right). \]

(19)

From (18) we find that for small values of \( V_{ds} << n V_T \)

\[ R_{\text{end}} \equiv \frac{V_{ds}}{i} = \frac{R_{ch}}{2} + R_s. \]

(20)

Furthermore

\[ R'_{\text{end}} \equiv \frac{dV_{ds}}{di} = \frac{R_{ch}}{2} + R_s = R_{\text{end}}. \]

(21)

Equation (16) for \( v_d \rightarrow 0 \) may be written as

\[ y = v_d + \ln \left[ v_d \left( 1 - \frac{v_d}{6} \right) \right] = \ln l_0 + \ln 2. \]

(22)

From (18) and (22) we find, in agreement with [8]

\[ \frac{dV_{gs}}{di} \approx \frac{R_{ch}}{6} + \frac{n V_T}{I_g}. \]

Equation (23) may be written as

\[ R'_{\text{end}} \equiv \frac{dV_{gs}}{di} = \frac{R_{ch}}{6} + \frac{n V_T}{I_g} + \frac{R_s + R_g}{I_g}. \]

(23)

In [7], it was incorrectly stated that

\[ \frac{dV_{gs}}{di} = \frac{R_{ch}}{2} + \frac{n V_T}{I_g}. \]

In a general case of an arbitrary gate current, (20), (21), and (23) may be rewritten as

\[ R_{\text{end}} = \alpha(i) \cdot R_{ch} + R_s \]

\[ R'_{\text{end}} = \alpha'(i) \cdot R_{ch} + R_s \]

(25)

\[ \frac{dV_{gs}}{di} = \frac{R_{ch}}{6} \cdot I_g + n V_T \left( \frac{I_0 - I_g}{I_g} \right) + R_g \cdot I_g \]

(26)

\[ R_{\text{end}} = \alpha(i) \cdot R_{ch} + R_d \]

\[ R'_{\text{end}} = \alpha'(i) \cdot R_{ch} + R_d \]

(39)

\[ \frac{dV_{gs}}{di} = \frac{R_{ch}}{6} \cdot I_g + n V_T \left( \frac{I_0 - I_g}{I_g} \right) + R_g \cdot I_g \]

(40)

\[ R_{\text{end}} = \alpha(i) \cdot R_{ch} + R_d \]

\[ R'_{\text{end}} = \alpha'(i) \cdot R_{ch} + R_d \]

(41)

\[ \frac{dV_{gs}}{di} = \frac{R_{ch}}{6} \cdot I_g + n V_T \left( \frac{I_0 - I_g}{I_g} \right) + R_g \cdot I_g \]

(42)

where \( \alpha(i), \alpha'(i), \) and \( \alpha''(i) \) are universal functions of \( i = I_g \cdot R_{ch}/n V_T \) [8]. For large \( v_d \gg 1 \left( V_{ds} \gg n V_T \right) \) we find

\[ \alpha(i) \approx \frac{2}{i} \ln \left( \frac{i + 2}{i} \right) \]

(28)

\[ \alpha'(i) \approx \frac{2}{(i + 2)} \]

(29)

and

\[ \alpha''(i) \approx \frac{1}{i}. \]

(30)

For small \( v_d \ll 1 \left( V_{ds} \ll n V_T \right) \)

\[ \alpha(i) \approx \frac{1}{i} \quad \frac{1}{24} \]

(31)

\[ \alpha'(i) \approx \frac{1}{i} \quad \frac{1}{12} \]

(32)

\[ \alpha''(i) \approx \frac{1}{i} \quad \frac{11}{3} \quad \frac{144}{i}. \]

(33)

Equations (28)-(30) apply for \( i > 15 \), (31)-(33) apply for \( i \ll 0.5 \). In the intermediate range of currents \( 0.5 < i < 15 \) the following expressions interpolate \( \alpha, \alpha', \) and \( \alpha'' \):

\[ \alpha(i) = \frac{1}{2} \quad \frac{1}{2 + 0.166i - 3.12 \times 10^{-4} i^2} \]

(34)

\[ \alpha'(i) = \frac{1}{2} \quad \frac{1}{2 + 0.3478 i + 7.72 \times 10^{-3} i^2} \]

(35)

\[ \alpha''(i) = \frac{1}{3} \quad \frac{1}{3 + 0.636i + 1.75 \times 10^{-2} i^2} \]

(36)

From (16) we find

\[ V'_{gs} = V_{ds} \cdot \frac{R_{ch}}{6} \cdot I_g + n V_T \ln \left( \frac{I_0 - I_g}{I_g} \right) + R_g \cdot I_g \]

(37)

and

\[ V'_{gs} = V_{ds} + n V_T \ln \left( \frac{I_0 \cdot \pi^2}{2 I_g} \right) + R_g \cdot I_g \]

(38)

for the small and large gate currents, respectively. Here \( I_g = J_{gs} \cdot W \cdot L \) and \( I_0 = n V_T/R_{ch} \). If the drain contact is grounded and the source contact is floating, then

\[ R_{\text{end}} = \alpha(i) \cdot R_{ch} + R_d \]

(39)

\[ R'_{\text{end}} = \alpha'(i) \cdot R_{ch} + R_d \]

(40)

\[ \frac{dV_{gs}}{di} = \frac{R_{ch}}{6} \cdot I_g + n V_T \left( \frac{I_0 - I_g}{I_g} \right) + R_g \cdot I_g \]

(42)
and

$$V_{gd} = V_{gd}^0 + nV_T \ln \left( \frac{I_g}{I_g^0} \right) + R \cdot I_g.$$  \hspace{1cm} (43)

The computed and analytical dependences of $\alpha$, $\alpha'$, and $\alpha^\delta$ on $i$ agree with better than 1 percent accuracy (see Fig. 2). These curves also coincide with the curves published in [8]. Equations (37) and (38) confirm the validity of the Fukui method because

$$\left( \frac{V_{gd}^*}{I_g} \right) - \left( \frac{V_{gd}^0}{I_g} \right) = \frac{V_{dr}^*}{I_g} - \frac{V_{dr}^0}{I_g} = R_s - R_d.$$  \hspace{1cm} (44)

As can be seen from (25) and (39) and “end” resistance measurements may be also used to determine $R_s = R_d$

$$R_{end} = R_{end}^* = R_s = R_d.$$  \hspace{1cm} (45)

Equations (25) and (39) offer a new interpretation of the “end” resistance measurements, which is quite different from the conventional approach (see (2)). In Section III this equation will be used to deduce the series resistance of ion-implanted GaAs FET's and the results will be compared with the modified Fukui method. We should notice that the value of $\alpha$ in (3) does not have to be known in order to determine $R_s$ and $R_d$.

We may also propose a simple measurement to determine the value of $R_s + R_d + R_{ch}$ independently from the “end” resistance measurements. The idea is to bias the drain contact slightly so that the drain current $I_d$ is now flowing, but $I_d << I_g$. In this case the drain current does not appreciably change the potential distribution in the channel and the source-drain voltage may be found from the superposition principle

$$V_{ds} = (R_s + R_d + R_{ch}) I_d + \left( R_s + \frac{R_{ch}}{2} \right) I_g.$$  \hspace{1cm} (46)

Hence, we may determine $R_s + R_d + R_{ch}$ from the intercept of $V_{ds}$ versus $I_g$ curve with the small drain current or, alternatively, as a slope of $V_{ds}$ versus $I_d$ curve with the gate current $I_g \gg I_d$. Also we find using (37)

$$V_{gs} = nV_T \ln \left( \frac{I_g}{I_g^0} \right) + \left( R_s + \frac{R_{ch}}{3} + R_g \right) \cdot I_g + \left( R_s + \frac{R_{ch}}{3} \right) \cdot I_d.$$  \hspace{1cm} (47)

A similar approach to the determination of $R_s$ and $R_d$ was recently discussed in [6] where (46) was derived. In this reference, however, the following equation was used for $V_{gs}$

$$V_{gs} = nV_T \ln \left( \frac{I_g}{I_g^0} \right) + (R_s + R_g) \cdot I_g + R_s \cdot I_d.$$  \hspace{1cm} (48)

As seen from the comparison of (47) and (48) two terms $nV_T \ln \left( \frac{I_g}{I_g^0} \right)$ and $R_{ch}/3 \cdot (I_g + I_d)$ are missing in (48) used in [6]. These terms may lead to a considerable error in the method of the $R_s$ determination in [6].

III. MEASUREMENT OF THE SERIES RESISTANCES OF ION-ImplANTED GaAs FET'S

GaAs MESFET's with 1.3-μm gate length were fabricated using multiple selective ion implantation into undoped LEC semi-insulating GaAs. Selenium ions were implanted in the active channel. Sulfur ions were implanted under ohmic contacts and Schottky diodes. The energy and dose were 200 keV and 2.2 X 10¹² cm⁻². The implantation range was 690 Å. Ohmic contacts were made using AuGe/Ni. The Schottky-barrier first-level metal was TiW/Au patterned using a dielectric assisted by lift-off technique. The interlevel dielectric was plasma-enhanced CVD silicon oxy-nitride, and the second-level metal was TiW/Au patterned using ion-beam milling. The drain-source spacing was 5 μm. The devices with gate widths of 20 and 40 μm were fabricated. The threshold voltage was close to −1 V.

The plot of the total resistance as a function of $1/I_d$ for the device with $W = 20$ μm was obtained in [2]. Here $g$ is the channel conductance at the given $V_{gs}$. From this measurement we obtained $R_s + R_d = 108 \Omega$, and the slope $L/W = 0.066$ which is in good agreement with $L/W$ ratio of 0.065 for this device determined by the direct optical measurement. The measured end resistances from the $V_{dr}$ versus $I_g$ curves for the floating drain with the source grounded and for the floating source with the drain grounded are

$$R_s + \frac{R_{ch}}{2} = 102.6 \Omega,$$  \hspace{1cm} (49)

and

$$R_d + \frac{R_{ch}}{2} = 126.3 \Omega.$$  \hspace{1cm} (50)

(See Fig. 3(a)). Hence, $R_d + R_s = 23.7 \Omega$ and $R_d = 65.8 \Omega$. $R_s = 42.2 \Omega$, $R_{ch} = 121 \Omega$. The sheet resistance of our material is estimated to be around 1420 Ω/square, leading to a full channel resistance of 92 Ω which is less than the measured one. The channel resistance is increased by the partial depletion under the gate.

The plots of $dV_{gs}/dI_g$ versus $1/I_d$ yield

$$R_s + \frac{R_{ch}}{3} + R_g = 107 \Omega.$$  \hspace{1cm} (51)
fabricated using a similar ion-implantation technique. We deduced the reasonable values of the source, drain, and gate resistances even though the small values of resistances made the measurements more difficult (see Fig. 3(b)).

The electron saturation velocity can be deduced from end resistance measurement as proposed in [9]. The values of $\alpha$ first decrease with the increase in $V_{ds}$ as predicted by the theory (see Fig. 2). With a further increase in $V_{ds}$, however, the values of $\alpha$ increase sharply. When the voltage drop $V_{ds}$ becomes comparable with $F_0 \cdot L_{eff}$ where $F_0$ is the velocity saturations field and $L_{eff} = \alpha \cdot L$ is the effective length of the section of the channel carrying the gate current, the electron velocity in this section of the channel saturates leading to the increase of the end resistance $R_{end}$ and, hence, to the increase in the measured value of $\alpha$. The value of $F_0$ can be estimated from $F_0 = (V_{ds})_{min}/(a_{min} \cdot L)$ where $a_{min}$ is the minimum value of $a$ and $(V_{ds})_{min}$ is the corresponding value of $V_{ds}$.

We measured the low-field mobility $\mu$ in our samples using the technique described in [2] and found $\mu \approx 2500 \, \text{cm}^2/\text{V} \cdot \text{s}$. We then estimated $v_s = \mu \cdot F_0$ and obtained the saturation velocity for our devices varying from 1 to $1.3 \times 10^5 \, \text{m/s}$.

If the gate current $I_g$ becomes larger than $F_0 \cdot L_{eg}/R_s$, where $L_{eg}$ is the source to gate spacing, the electron velocity may saturate in the source to gate spacing, invalidating our technique.

This condition may be also rewritten as

$$I_g > \frac{F_0}{\mu} \cdot \frac{L_{eg}}{R_s} \quad (53)$$

In our devices $v_s \approx 1.2 \times 10^5 \, \text{m/s}, L_{eg} \approx 1.3 \, \mu\text{m}, \mu = 2500 \, \text{cm}^2/\text{V} \cdot \text{s}, R_s = 42.2 \, \Omega$, and $I_{eg} \approx 14.8 \, \text{mA}$ well above the maximum gate current of 5-6 mA used in the measurement (see Fig. 2).

### IV. Conclusion

Both the Fuku method (modified to include the nonuniform doping and mobility profiles) and the “end” resistance measurement technique allow an accurate determination of series source, drain, and gate resistances in ion-implanted GaAs FET’s. Also we proposed a simple and convenient method for the in situ determination of the electron saturation velocity using the “end” resistance measurements. The technique described in this paper accurate enough to be utilized for parameter acquisition and device characterization of GaAs FET’s. It may also
be applied to other solid-state devices such as MOSFET’s or modulation-doped field-effect transistors.

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References


