The Impact of Semiconductor Technology Scaling on CMOS RF and Digital Circuits for Wireless Application

Kwyro Lee, *Senior Member, IEEE*, Ilku Nam, *Student Member, IEEE*, Ickjin Kwon, *Member, IEEE*, Joonho Gil, *Member, IEEE*, Kwangseok Han, *Member, IEEE*, Sungchung Park, *Student Member, IEEE*, and Bo-Ik Seo, *Student Member, IEEE*

***Abstract*—The impact of CMOS technology scaling on the various radio frequency (RF) circuit components such as active, passive and digital circuits is presented. Firstly, the impact of technology scaling on the noise and linearity of the low-noise amplifier (LNA) is thoroughly analyzed. Then two new circuits, i.e., CMOS complementary parallel push-pull (CCPP) circuit and vertical-NPN (V-NPN) circuit for direct-conversion receiver (DCR), are introduced. In CCPP, the high RF performance of pMOS comparable to nMOS provides single ended differential RF signal processing capability without the use of a bulky balun. The use of parasitic V-NPN bipolar transistor, available in triple well CMOS technology, has shown to provide more than an order of magnitude improvement in $1/f$ noise and dc offset related problems, which have been the bottleneck for CMOS single chip integration. Then CMOS technology scaling for various passive device performances such as the inductor, varactor, MIM capacitor, and switched capacitor, is discussed. Both the forward scaling of the active devices and the inverse scaling of interconnection layer, i.e., more interconnection layers with effectively thicker total dielectric and metal layers, provide very favorable scenario for all passive devices. Finally, the impact of CMOS scaling on the various digital circuits is introduced, taking the digital modem blocks, the various digital calibration circuits, the switching RF power amplifier, and eventually the software defined radio, as examples.**

***Index Terms*—CMOS scaling, digital RF, integrated passives, RF CMOS, wireless digital circuits.**

I. Introduction

RECENTLY, we have seen a widespread variety of mobile computing and communication services. Based on the Edholm's law of bandwidth, which is the exponential law of telecommunication data rates versus year, being equivalent to Moore's law in semiconductors, it is predicted that all telecommunication will eventually become both wireless and mobile [1]. The driving force for this is the low cost and low power consumption provided by the continuous semiconductor technology scaling. Therefore, it is now time to see how the semiconductor technology scaling influences future wireless circuits and systems. In Section II, the impact of active device scaling on radio frequency (RF) active circuits as well as transceiver architectures will be introduced. Then the impact of technology scaling on various passive devices will be discussed in Section III, which is as important as the active ones for RF circuits. In Sections IV and V, the impact of device scaling for digital baseband as well as digital RF circuits will be illustrated, followed by the Conclusion.

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K. Lee, I. Nam, S. Park, and B.-I. Seo are with the Department of Electrical Engineering and Computer Science and MICROS Research Center, Korea Advanced Institute of Science and Technology, Daejeon 305-701, Korea (e-mail: krlee@ee.kaist.ac.kr).

I. Kwon is with Samsung Advanced Institute of Technology, Kyunggi, Korea.

J. Gil is with RadioPulse Inc., Songpa-gu, Seoul 138-711, Korea.

K. Han is with RF/Analog PT, System LSI Division, Samsung Electronics Company, Ltd., Kyunggi 449-711, Korea.

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II. Impact of Active Device Scaling on RF Active Circuits and Systems

The simplicity of the following MOSFET drain saturation current ($I_{\rm dsat}$) equation has contributed greatly to integrated circuit technology development

$$I_{\rm dsat} = \mu C_{\rm ox}\left(\frac{W}{L}\right)(V_{\rm gs} - V_{\rm gs})^2. \tag{1}$$

In (1), μ is the mobility, $C_{\rm ox}$ is the unit area gate oxide capacitance, W is the channel width, and L is the channel length, $V_{\rm gs}$ is the gate-to-source voltage, and $V_{\rm gs}$ is the threshold voltage. In scaled CMOS, due to the mobility degradation by vertical as well as lateral electric fields, (1) reduces to the following simple equation with reasonable accuracy:

$$I_{\rm dsat} \approx WK(V_{\rm gs} - V_{\rm gs}). \tag{2}$$

Here, K is a constant that is technology dependent. Equation (2) states that g_m is a constant independent of channel length as well as gate overdrive voltage. In RF circuits, interfacing off-chip components such as antennas and filters, the impedance level should be determined at $\rm Z_o$ of 50 Ohm. Thus transistor width is chosen so as to satisfy the desired impedance level. Once transistor width is chosen in this way, we obtain the following scaling rule:

$$C_{\rm gs} \sim \lambda \quad f_T \sim \frac{1}{\lambda} \quad f_{\max} \sim \frac{1}{\lambda}. \tag{3}$$

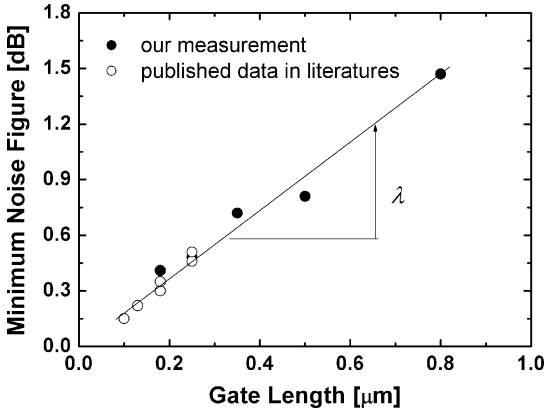

Fig. 1. $\mathrm{NF_{min}}$ at 2.4 GHz versus gate length. Solid dots are obtained from fabricated devices using standard 0.18-μm technology and open dots are from [3].

Here, λ is the technology-scaling factor. According to Fukui [2], however, the minimum noise figure of a FET can be expressed as

$$NF_{\min} \sim 1 + \frac{K_f f}{f_T}. \tag{4}$$

In (4), K_f is a constant called Fukui parameter. Equations (3) and (4) state that $NF_{\min}$ scales as λ in dB scale, which is verified as shown in Fig. 1. It is very interesting to notice that Fukui's formula, which is an empirical formula originally proposed for GaAs MESFET in the 1970s, works remarkably well even for deep-submicron MOSFET.

In a low-noise amplifier (LNA) circuit, as input matching is deviated from noise optimum point, the noise figure increases as follows:

$$NF = NF_{\min} + \frac{R_n}{G_S} \cdot (Y_S - Y_{\mathrm{opt}})^2. \tag{5}$$

Here, R_n is the equivalent input noise resistance, $Y_S (= G_S + jB_S)$ is the complex source admittance, and Y_{opt} is the complex optimal noise admittance. Note that the noise parameters include the small-signal parameters as well as the physical noise source [4].

Although the improvement of $NF_{\min}$ due to scaling is shown in Fig. 1, for practical purposes it should be collaborated with the scaling of the noise resistance because R_n indicates how sensitively the noise performance deviates from the optimal value. From (5), we can easily see that $R_n \sim \lambda$ and $Y_{\mathrm{opt}} \sim 1/\lambda$, which indicates optimum noise matching becomes much more sensitive to source impedance mismatch by $1/\lambda$ times, while the noise circle becomes broader by $1/\lambda^2$ times. The former is quite an unfavorable scaling scenario. However, scaling of $R_n \sim \lambda$ indicates a very small noise figure increase when input matching deviates from the optimally matched condition. This indicates that noise figure of scaled down device is very insensitive to source impedance mismatch, leading to a very favorable scenario. This insensitiveness of noise figure on input source matching condition would make LNA circuit design much easier. Fig. 2 shows another insensitiveness of scaling on noise figure. $NF_{\min}$ for scaled CMOS is very immune to the gate-to-source bias change. It is also worth noticing that

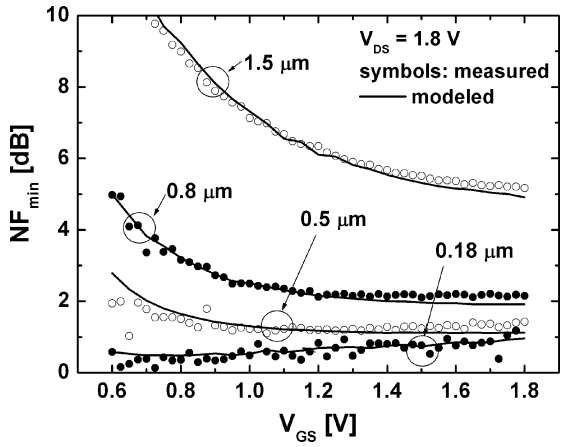

Fig. 2. $\mathrm{NF_{min}}$ at 2.4 GHz versus gate-to-source bias voltage.

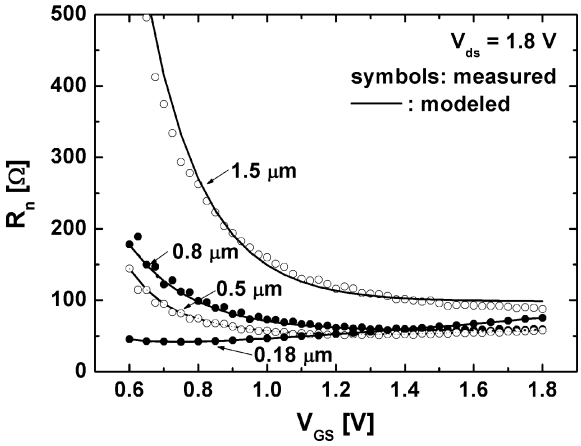

Fig. 3. Noise resistance, R_n, as a function of V_{GS} for the devices with various gate lengths.

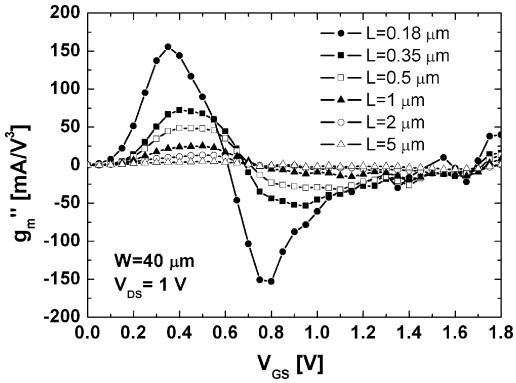

Fig. 4. g_m'' versus gate-to-source bias voltage. This data is obtained from fabricated devices using standard 0.18 μm technology.

the noise resistance R_n becomes very insensitive to gate bias change as shown in Fig. 3. Note here that the modeled values of $NF_{\min}$ and R_n in Figs. 2 and 3 are calculated ones by thermal noise models recently developed for short-channel MOSFETs [4], [5].

On the other hand, the linearity of RF circuits is very important circuit performance issue for wireless communication systems. In RF CMOS, most of the nonlinearity is due to that in the transconductance. In Fig. 4, we plot second derivatives of nMOS

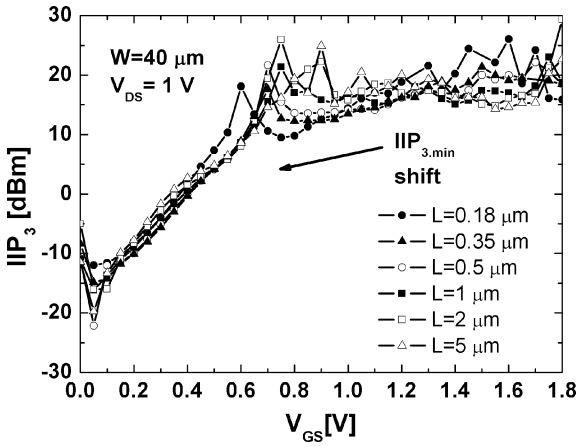

Fig. 5. IIP_3 versus gate-to-source bias voltage. This data is calculated from g_m'' data in Fig. 4.

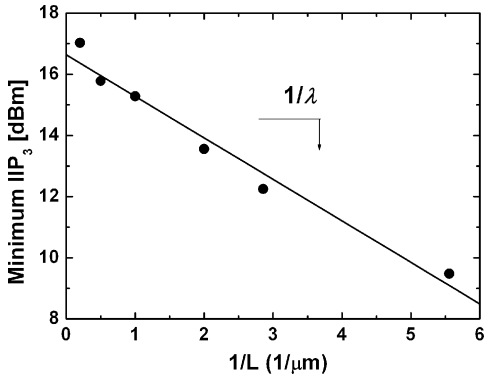

Fig. 6. IIP_3 versus inverse channel length for the devices shown in Fig. 5.

transconductance measured for 0.18-μm CMOS devices. Fig. 5 shows the IIP_3 calculated with the second derivatives of nMOS transconductance in Fig. 4. In Fig. 6, we plot the IIP_3 in moderate inversion which is most popularly used bias point for LNA, versus channel length. It shows adverse scaling scenario, unfortunately. Note, however, that there are many ways to improve this for scaled CMOS circuits using various feed-forward and/or feedback techniques. The use of linear superposition of several FETs with different channel width biased at different gate and/or substrate bias is a good example of feed-forward techniques [6], [7]. On the other hand, higher RF performance expected from scaled down transistors permits us to use various desensitizing negative feedback techniques, allowing us to trade-off various circuit performances such as gain and linearity. These include source inductor degeneration, gate-to-source capacitor degeneration, resistive shunt feedback, and so forth [8], [9]. This is very similar to an operation amplifier circuitry with negative feedback, where closed loop circuit transfer characteristics are very linear because they are determined by passive feedback components, sacrificing infinite gain of operational amplifier.

In CMOS technology, nMOS is mostly used for RF applications due to its superior performance. In scaled CMOS, however, pMOS also has good small-signal RF performance, as shown in Fig. 7 [10]–[13]. As a result, pMOS combined with NMOS, can be used in push-pull RF circuits as shown in Fig. 8(a) [14]. Fig. 8(b) illustrates how the complementary CMOS parallel push-pull (CCPP) circuit gives a push-pull

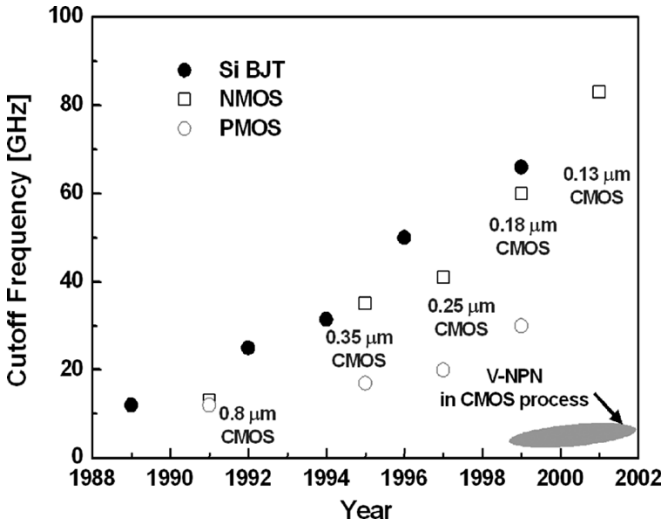

Fig. 7. State-of-the-art transistor cutoff frequency versus year. Data are from [10]–[13].

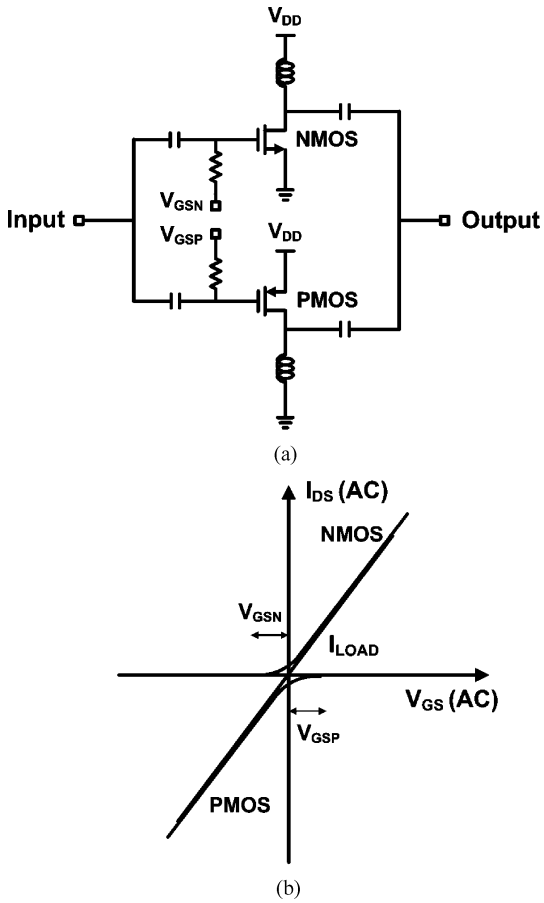

Fig. 8. (a) CCPP amplifier schematic diagram and (b) AC I-V curve of CCPP amplifier.

action. In CMOS push-pull RF circuits, highly symmetric differential circuit action is feasible without the use of a bulky balun, providing very good IIP_2 performance as well as large isolation. In the resistive mixer using pMOS combined with NMOS, our experimental results show more than an order of magnitude improvement in IIP_2 and port isolation performances as shown in [15]. The complementary characteristics

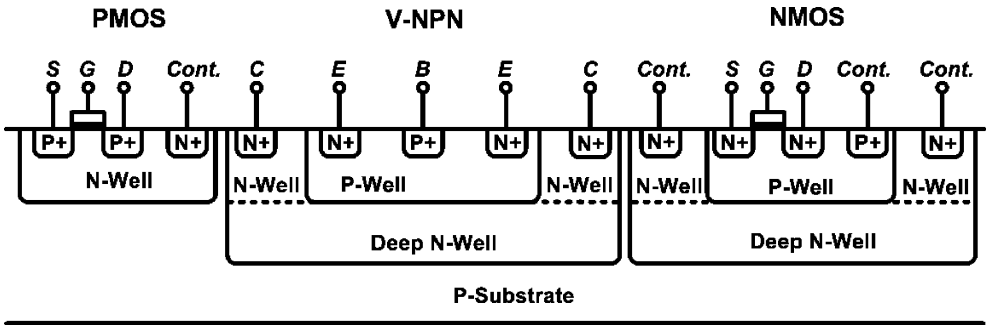

Fig. 9. Cross-sectional view of the triple-well CMOS technology, providing parasitic V-NPN.

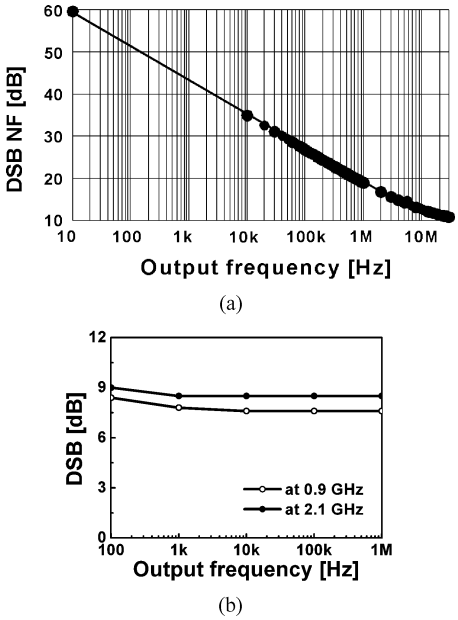

Fig. 10. Noise figure for: (a) nMOS mixer (calculated) and (b) V-NPN mixer (measured from chip fabricated using TSMC 0.18 μm CMOS technology) [13].

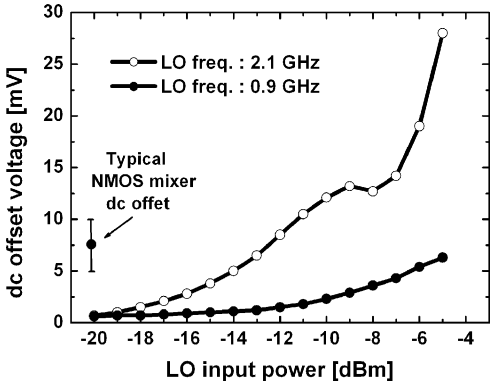

Fig. 11. Measured dc offset from nMOS and V-NPN mixer. The latter gives an order of magnitude improvement [13].

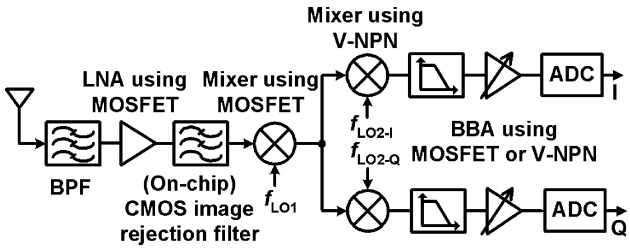

Fig. 12. Single-IF DCR receiver using V-NPN in second mixers, greatly relaxing the frequency limitation of V-NPN.

of nMOS and pMOS can indeed be fully utilized in RF core circuits without significantly degrading RF performance.

Nowadays, most of the deep submicron CMOS technology adopts deep triple n-well process, which provides parasitic vertical-NPN (V-NPN) bipolar junction transistor as shown in Fig. 9. As shown in Fig. 7, because the unit current gain cutoff frequency of parasitic V-NPNs can be from 600 MHz to several gigahertz, the parasitic V-NPN can be a very useful device option in the design of analog and RF CMOS circuits. By combining V-NPN and MOSFET devices on the same chip, we can optimize the analog/digital circuits as shown in the following example.

Fig. 10 shows the noise performance of nMOS Gilbert mixer and V-NPN Gilbert mixer, respectively. The V-NPN mixer has excellent low-frequency noise performance, showing only thermal noise and almost $1/f$ noise-free characteristic. On the contrary, as shown in Fig. 10(a), the low-frequency noise performance of nMOS Gilbert mixer is deteriorated by $1/f$ noise. Fig. 11 also shows the output dc offset voltage of V-NPN mixer measured as a function of local oscillator (LO) input power, zero-power limit of which is 0.6 mV. On the other hand, typical value for that of nMOS mixer is measured as 5–10 mV. Consequently, V-NPN can provide superb solution to inherent problems of CMOS direct-conversion receiver (DCR) such as $1/f$ noise and dc offset and can open a new horizon for CMOS implementation of DCR [13].

As the triple n-well CMOS technology scales down, the cutoff frequency of V-NPN is expected to improve because the base width of V-NPN will be thinner. It should be noted here, however, that the use of parasitic V-NPN in existing CMOS technology should be limited for low frequency RF circuits because its unit current gain cutoff frequency is an order of magnitude lower than that of CMOS. One such example is the dual conversion zero-IF receiver shown in Fig. 12. Here V-NPN is adopted in the zero-IF DCR mixer and baseband analog (BBA) circuits, whose operating frequency is much lower than that of the RF signal from an antenna [13].

III. Impact of CMOS Scaling for Passive Devices

In CMOS scaling, both active devices and lowest interconnection line scale down, which is called forward scaling. However, top-level metallization scales inversely; n other words, top

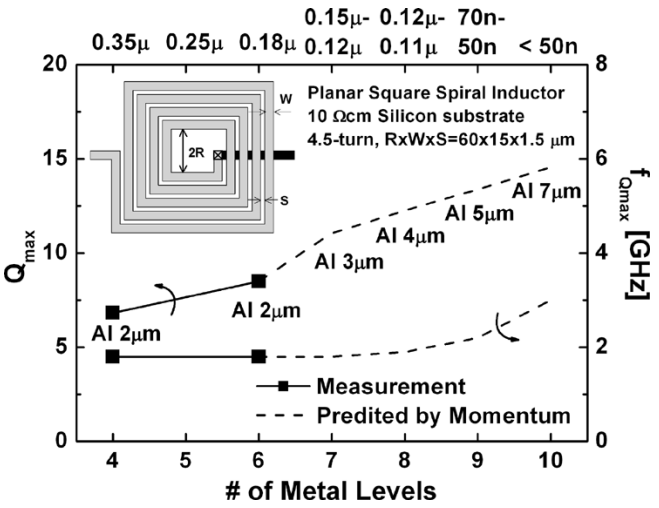

Fig. 13. Integrated inductor quality factor and the corresponding frequency versus number of interconnection layers. The solid squares are measured from chip fabricated using TSMC 0.18 μm technology and the dashed lines are calculated from scaled CMOS technology scaled following SIA load map [17].

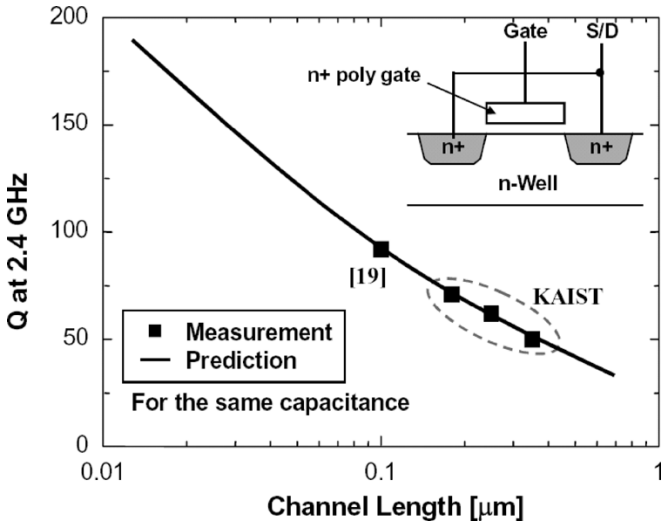

Fig. 14. Accumulated type MOS varactor quality factor scaling. The solid squares are measured from TSMC 0.18-μm technology and the solid line is the calculated one.

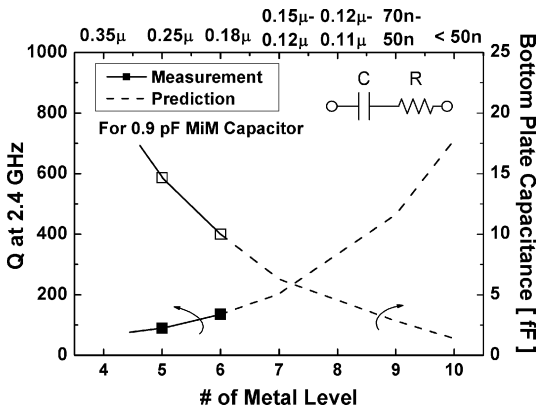

Fig. 15. Quality factor and parasitic bottom plate capacitance scaling for 0.9-pF MIM capacitors. The squares are measured from TSMC 0.18-μm technology and the solid and dashed lines are calculated ones.

metal thickness as well as total dielectric insulator thickness becomes thicker, both of which are indispensable for increasing the quality factor of an integrated inductor [16]. These combined with better transistor scaling, therefore, will lead all the passive devices performance to scale favorably. For example, inductor will have smaller parasitic capacitance to substrate, varactor's quality factor will be better, and switched capacitor will have much better quality factor, all in a favorable direction, as shown from Figs. 13–16, respectively. The predicted and calculated values were based on both the SIA roadmap [17] and the accurate RF models found in [18], [20], and [21].

Fig. 13 predicts the integrated inductor quality factor and the corresponding frequency versus number of interconnection layers. As depicted in Fig. 13, the thicker top metal leads to an improvement in the quality factor. Furthermore, together with lower dielectric constant and farther top-level to substrate distance, the great reduction of the substrate loss and parasitics results in the significant improvement of quality-factor [18]. Cu interconnect technology will replace current Al technology gradually, and therefore the performance of on-chip inductors will improve greatly. However, inductance will not scale as transistor. In other words, silicon areas being occupied by on-chip inductors will not scale down even though CMOS technology advances.

Fig. 14 shows the quality factor scaling of an accumulated-type MOS varactor. The equivalent capacitance of the MOS varactor is the sum of variable gate capacitance and fixed overlap capacitance [20]. The dominant contribution of the series equivalent resistance is the channel resistance. Because the channel resistance scales down as the channel length scales, the quality factor will increase significantly. In addition, the gate-oxide thickness also scales down, and so the layout density will improve.

Fig. 15 shows the quality factor and parasitic bottom plate capacitance scaling for the MIM (metal-insulator-metal) capacitor [21]. To inspect the scaling properties of the MIM capacitor, the physical MIM capacitor model [21] is simplified to the equivalent series R and C model as shown in the insert of Fig. 15. The equivalent R and C are [22]

$$R = \frac{\rho \cdot K(t_m)}{A} \tag{6}$$

and

$$C = \frac{\varepsilon A}{t_{\rm ox}} \tag{7}$$

where $K(t_m)$ is a factor for the contact resistance to the metal, ρ is the top-metal resistivity, A is the area, ε is the dielectric constant, and $t_{\rm ox}$ is the dielectric thickness. From (6) and (7), the resulting Q is

$$Q = \frac{1}{\omega CR} = \frac{1}{\left(\frac{\varepsilon}{t_{\rm ox}}\right) \cdot \rho K(t_m)}. \tag{8}$$

The MIM capacitor density, i.e., capacitance per unit area, increases slightly [22]. But, because the metal resistivity (ρ) decreases greatly and the substrate parasitics reduces as shown in Fig. 15, the quality factor of MIM capacitor will be better.

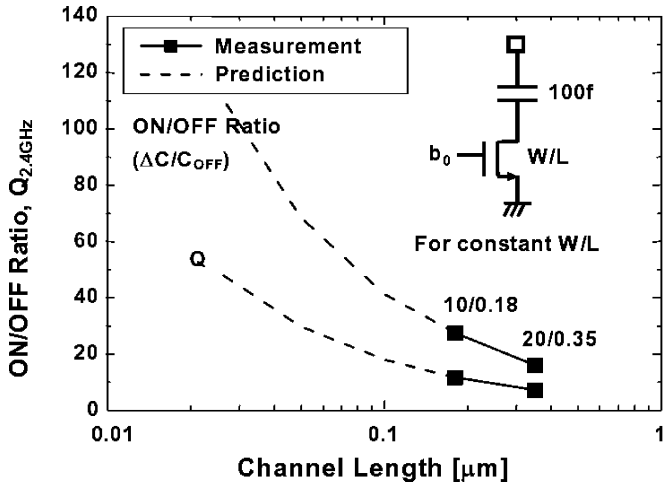

Fig. 16. On-off impedance ratio and quality factor of scaled switched capacitors at 2.4 GHz. The squares are measured from TSMC 0.18-μm technology and the solid and dashed lines are calculated ones.

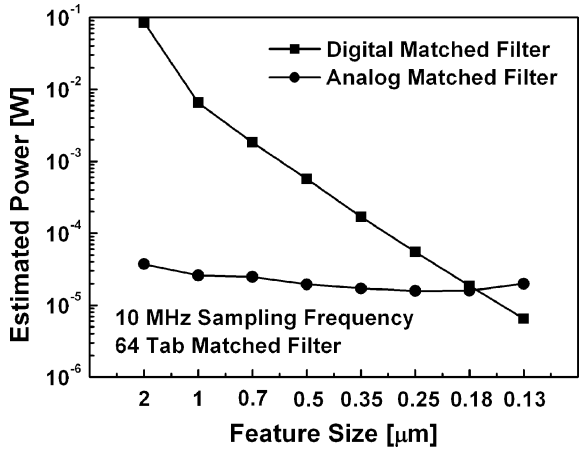

Fig. 17. Calculated power consumption comparison between digital and analog matched filer. This is calculated following the model assumed in [24].

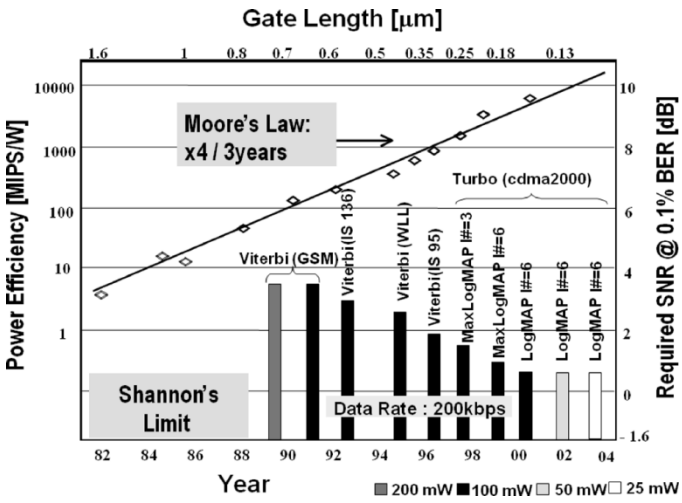

Fig. 18. Impact of Moore's Law in achieving Shannon's limit with affordable power consumption. This figure shows that Moore's law at 0.13-μm technology allows us to achieve 2.1-dB sensitivity away from Shannon's limit of -1.6 dB at only 25-mW power consumption [26]–[28].

Fig. 16 shows the on/off impedance ratio and quality factor of scaled switched capacitors at 2.4 GHz. The performance of scaled switched capacitors will improve because they consist of both better transistor and MIM capacitor as scaling continues.

Consequently, all passive devices scale in a favorable direction as CMOS technology scales down. Because the power consumption of RF/microwave circuits is largely affected by the performance of passive devices, the scaling of passive devices is advantageous in low-power circuit design. For example, one of the key design issues in the low phase noise and low power VCO (voltage-controlled oscillator) is how to design and optimize the tank inductor and varactors [23].

IV. Impact of CMOS Scaling for Digital Baseband Circuitry

Because digital signal processing provides inherent accuracy (6 dB/bit and ppm accuracy of clock), adaptability, flexibility, and programmability, we see more and more digital circuitry in modern radio. These allow sophisticated signal processing, which enables a radio to obtain selectivity and sensitivity up to Shannon's limit, and auto calibration (trimming) for RF/IF/BBA analog circuit imperfections, and so forth. Fig. 17 shows that power consumption for the digital matched filter scales down very fast as technology scales while the analog matched filter does not scale and there is a crossover at 0.18 μm for this particular circuit example. These calculations were done using the formula developed in [24]. In this example, the scaling effect on the power consumption of the analog matched filter is rather independent of process technology. The great power reduction like the digital matched filter cannot generally be achieved in the analog matched filter. Fig. 18 shows how Moore's law helps us to obtain the Shannon's limit with affordable power consumption in hand-held phones. The data shown in Fig. 18 is calculated based on the following assumption: the data rate is 200 kbps and only a single digital signal processor (DSP) is available to carry out to the decoding of forward error correction (FEC) codes such as several convolutional codes or turbo codes. As shown in Fig. 18, the power efficiency of DSP is exponentially increasing by a factor of 4 every three years [25]. Consequently, given limited power consumption budget, CMOS scaling allows us to obtain the well-known Shannon's limit [26]–[28]. Note that the bars in Fig. 18 represent the differences of required signal-to-noise ratio (SNR) to obtain 0.1% bit error rate from the Shannon's limit of -1.6 dB. For example, the logarithmic maximum *a posteriori* (LogMAP) decoder for Turbo Codes being implemented in 0.13 μm CMOS technology with power consumption as low as 25 mW, requires the SNR approaching the Shannon's limit within 2.1 dB.

All RF circuits need calibration or trimming for manufacturing and temperature dependent circuit imperfections such as gain mismatch, phase mismatch, and nonlinearity, etc. This has traditionally been done in a laborious way using external measurement equipments, which make it very expensive and time consuming. CMOS, however, is the only technology that provides circuits and algorithm for measurement and correction as well as memory devices to store calibration data, and all the necessities for the automatic calibration for the circuit imperfections in a single chip. Thus, fully automated calibration or trimming is feasible in CMOS radio [29].

V. Impact of CMOS Scaling for Digital RF

As transistor speed becomes faster, completely new concepts of digital RF technology have been proposed. Among them, digital RF power amplifier and radio using ultra-wide band (UWB) signals are two notable examples.

As for the digital RF power amplifier, one of the most promising candidates is the switching mode power amplifier [30]. In conventional analog power amplifier, it is very difficult to obtain both high power efficiency and linearity at the same time. However, in switching mode power amplifier, 100% power efficiency without any signal distortion can theoretically be obtained. This is very similar to pulsewidth modulated (PWM) signal for audio power amplifier. Because it is digitally modulated, it is very programmable, too.

The UWB radio recently being standardized as 802.15.3a and 802.15.4a by IEEE is another interesting digital wireless communication concept [31]. Conventional radio has evolved from old narrow band radio, where the uses of high quality passive filters are preferred to those of transistors in obtaining sensitivity and selectivity requirement for multiple access communication. However, the success of CDMA system using direct sequence spread spectrum (DSSS) signal has opened the feasibility to remove some of narrow band filters by using wider bandwidth baseband signal. UWB is the extreme case where RF baseband digital signal is directly used for radio communication. Therefore, it is very suitable for being implemented using digital circuitry.

The above two examples indicate that we will see an all-digital radio in the near future, where all circuitry will be digital except for LNA and analog-to-digital converter (ADC). These radios, being digital, will be highly programmable, so that they can easily be configured by software, just like computers.

VI. Conclusion

Endless scaling of modern semiconductor technology has changed mobile hand-held radio system and service drastically during the last two decades. Soon everyone will carry billions of transistors in his mobile information terminal consuming only few hundreds of milliwatt power. In this paper, we showed that technology scaling helps continuously for us to design more smart systems in a less costly way. We will see all digital except RF LNA, mixer, and RF filter in the near future radio. Someday, we will have all digital radio except LNA and ADC, such as ideal software radio and ultra-wide band transceivers, where everything will be defined by software just like the computer at present.

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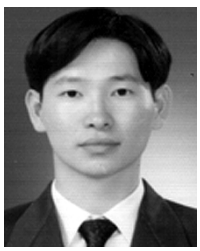
Kwyro Lee (M'80–SM'90) received the B.S. degree in electronics engineering from Seoul National University, Seoul, Korea, in 1976 and the M.S. and Ph.D. degrees from the University of Minnesota at Minneapolis-St. Paul in 1981 and 1983, respectively, where he performed pioneering work for characterization and modeling of AlGaAs/GaAs heterojunction field-effect transistors.

From 1983 to 1986, he was an Engineering General Manager with GoldStar Semiconductor Inc., Seoul, where he was responsible for the development of the first polysilicon CMOS products in Korea. In 1987, he joined the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, as an Assistant Professor in the development of electrical engineering. He is currently a Professor with KAIST. From 1998 to 2000, he served as the KAIST Dean of Research Affairs and the Dean of Institute Development and Cooperation. Since 1997, he has been the Director of the Micro Information and Communication Remote-object Oriented Systems (MICROS) Research Center, an Engineering Center of Excellence supported by the Korea Science and Engineering Foundation. In March 2005, he joined LG Electronics Institute of Technology, Seoul, as Executive Vice President. He has authored or coauthored over 150 publications in major international journals and conferences. He authored *Semiconductor Device Modeling for VLSI* (Englewood Cliffs, NJ: Prentice-Hall, 1993) and was one of the co-developers of AIM-SPICE, the world's first SPICE run under Windows.

Dr. Lee is a Life Member of the Korean Institute of Electrical and Communications Engineers. From 1990 to 1996, he served as the Conference Co-Chair of the International Semiconductor Device Research Symposium, Charlottesville, VA. From 1998 to 2000, he served as the Chairman of the IEEE Korea Electron Device Chapter and currently serves as an Elected Member of the Administrative Committee (AdCom) of the Electron Devices Society (EDS).

Ilku Nam (S'02) received the B.S. degree in electronic engineering from Yonsei University, Seoul, Korea, in 1999 and the M.S. degree in electrical engineering and computer science in 2001 from the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, where he is currently working toward the Ph.D. degree.

Since 2000, he has participated in the development of low-power radio frequency (RF) front-end circuits, low-power analog baseband circuits and the wireless system-on-a-chip (SOC) for low-rate wireless personal area network (LR-WPAN). His research interests include CMOS RF/analog IC and RF system design for wireless communication, and interfaces among RF, modems, and MAC layers.



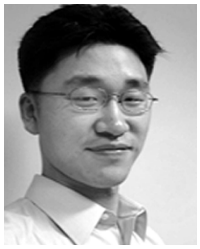
Ickjin Kwon (M'05) received the B.S., M.S., and Ph.D. degrees in electrical engineering and computer science from the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, in 1998, 2000, and 2004, respectively.

In 2004, he joined the Samsung Advanced Institute of Technology (SAIT), Kyunggi, Korea, where he is currently a Senior Research Engineer in the Communication and Network Lab. His research interests include radio frequency and baseband integrated circuits and systems for wireless communications.

Joonho Gil (S'98–M'04) received the B.S. and M.S. degrees in electrical engineering in 1997 and 1999, respectively, and the Ph.D. degree in electrical and computer science in 2003, all from the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, Korea.

He is currently with RadioPulse Inc., Seoul, Korea, where he has developed CMOS radio frequency (RF)-ICs for wireless applications. His research interests include CMOS RF/microwave integrated circuits for wireless communication and on-chip passive device modeling.

Dr. Gil received a Splendor Prize in the Samsung Humantech Paper Contest in 1999.



Kwangseok Han (S'99–M'05) received the B.S., M.S., and Ph.D. degrees in electrical engineering and computer science from Korea Advanced Institute of Science and Technology (KAIST), Daejeon, Korea, in 1998, 2000, and 2004, respectively.

Since 2004, he has been with Samsung Electronics, Kyunggi, Korea, as a radio frequency (RF) Circuit Designer. His research activities include nonvolatile nano-crystal memory, RF CMOS modeling, high-frequency thermal noise modeling, and RF circuits design.

Dr. Han received a Best Student Award for the Outstanding Paper in the Silicon Technology at the 1999 IEEE International Conference on VLSI and CAD and an Outstanding Paper Prize from Applied Materials, Inc. (Korea Branch) Paper Contest in 2001. He also received a Korea Foundation for Advanced Studies scholarship from 1999 to 2002.

Sungchung Park (S'02) was born in 1976. He received the B.S. and M.S. degrees in electrical engineering in 2000 and 2002, respectively, from the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, Korea, where he is currently working toward the Ph.D degree.

In 2003, he was with SPINCOM, University of Minnesota, Minneapolis, as a Visiting Researcher. Since 2004, he has been working on the design and implementation of next-generation WLAN systems (IEEE 802.11n). His research interests include communication theory and its VLSI implementation, focusing on high-rate wireless communications.

Bo-Ik Seo (S'01) was born in Daegu, Korea, 1977. He received the B.S. and M.S. degrees in electrical engineering in 1999 and 2001, respectively, from Korea Advanced Institute of Science and Technology (KAIST), where he is currently working toward the Ph.D. degree in electrical engineering.

His research interests include the digital system design for wireless communication systems and microprocessors.