K-Band FMCW Radar CMOS Front-End ICs with 13.3 dBm Output Power

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***Abstract* — This paper presents CMOS front-end ICs with 13.3 dBm output power for K-band FMCW radar, which is integrated in 0.13-µm CMOS technology. The transmitter consists of a voltage controlled oscillator, divider chain, power amplifier, and additional buffers. The receiver consists of a low-noise amplifier, IQ mixers, an IQ generator, and buffers. The leakage problem can be mitigated by adopting differential topology and ground shielding. As a result, the receiver achieves a conversion gain of 35.7 dB, a P1dB of -31.6 dBm, and a DSB noise figure of 5.5 dB. The transmitter achieves the tuning range of 23.8~24.5 GHz and the phase noise of -104 dBc/Hz @ 1MHz offset. The receiver and transmitter chips consume 121.5 mW and 373.5 mW from a 1.5 V power supply, respectively. Using these two chips, the K-band FMCW radar module is implemented and verified by measuring the distance of an object.**

***Index Terms* — CMOS, Frequency modulated continuous wave (FMCW), K-band, radar receiver, radar transmitter.**

I. Introduction

Since the Federal Communications Commission (FCC) allocated the frequency band of 24~24.25 GHz for long-range radar (LRR) systems, there have been many research efforts regarding frequency modulated continuous wave (FMCW) radar operating in this frequency range. However, to detect an object at long range, a lower noise figure and higher output power are required for higher signal-to-noise ratios (SNRs).

Because the number of the sensors has to be increased for the better reliability and more diverse operation, there have been some attempts to implement FMCW radar in CMOS technology for low cost [1-2]. However, the leakage of high output power can adversely affect the operation of injection-locking operating blocks, such as a VCO and a injection locking frequency divider, especially in CMOS technology that has lossy substrates. Therefore, previous works have limited output power of less than 10 dBm [1-2] and/or exclude injection-locking operation block in CMOS IC [1]. It is also difficult to verify radar operation with CMOS chipsets [2].

This paper presents the highest output power K-band FMCW radar front-end chipset fabricated using 0.13-µm CMOS technology to date. Leakage was minimized by using a fully differential topology throughout the whole system and shielding the leakage with a ground wall so that it could not affect the sensitive blocks. To verify the radar operation of the proposed CMOS chipset, a radar module was implemented, and it successfully measured the range of an object.

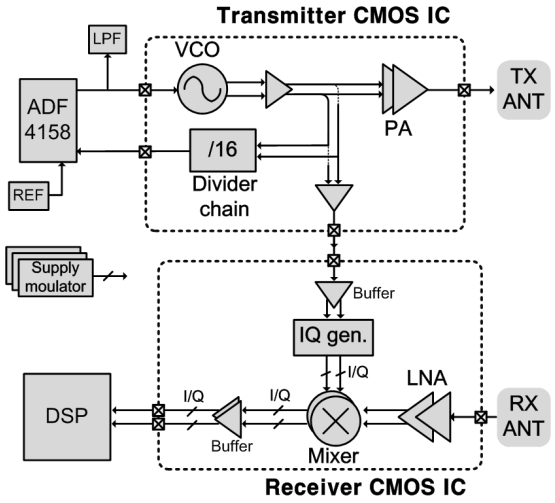


Fig. 1. Block diagram of the proposed FMCW radar transceiver module

II. FMCW Radar Transceiver Architecture

Fig. 1 shows a block diagram of the proposed FMCW radar transceiver. As previously mentioned, a high output power and low noise figure are required for accurate range measurement. For the high power, a power amplifier is included in the transmitter. Because the low noise amplifier can be adversely affected by leakage from the large output swing of the power amplifier block, we implemented the receiver and transmitter chips separately. VDD and bias are provided by the supply modulator. A phase-locked loop (PLL) is required to reduce the phase noise near the carrier frequency and synthesize a linear chirp. The PLL loop comprises a VCO and a divider chain of the CMOS transmitter chip together with the external frequency synthesizer chip ADF 4158. A local oscillator (LO) signal is provided to the receiver from the transmitter chip.

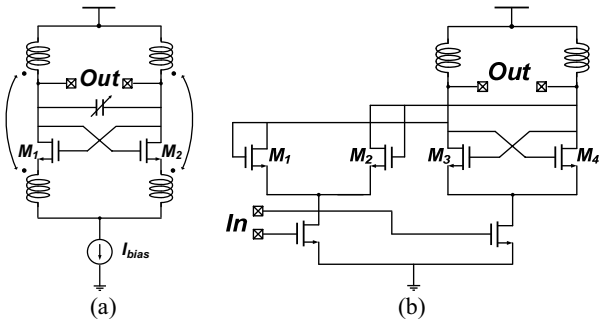


Fig. 2. Schematic of (a) the VCO and (b) the injection-lock divider (1st divider)

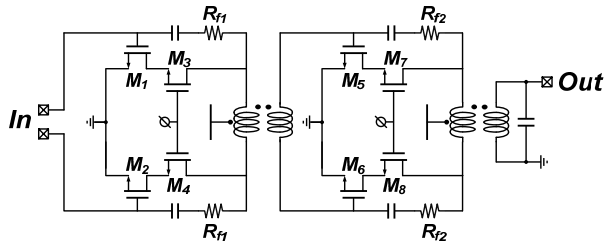


Fig. 3. Schematic of the power amplifier

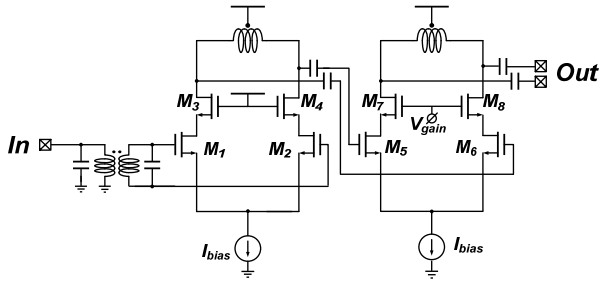


Fig. 4. Schematic of the low noise amplifier

III. Circuit Designs

A. Transmitter (Tx)

The transmitter comprises a voltage controlled oscillator (VCO), a divider chain, a power amplifier (PA) and an additional buffer. Fig. 2 (a) shows a schematic of the VCO. The drain-to-source feedback VCO topology is adopted. For low loss and a high quality factor, an asymmetric transformer is used [4].

The divide-by-16 frequency divider chain consists of four cascaded divide-by-2 frequency dividers. The 1st divider operates as an injection-locked divider, as shown in Fig. 2 (b), to reduce power consumption and enhance the output swing. The rest of the frequency divider chain adopts a conventional CML divider for compact layout.

The designed PA is shown in Fig. 3. It has two stages, namely the driver stage and power stage. Both have a differential cascode structure. The matching circuits are designed with a transmission line transformer. We insert the feedback resistors Rf1 and Rf2 into the driver stage and power stage, respectively, to ensure stability. To reduce leakage from the power amplifier, a ground wall, including all the metal and p-diffusion layers is used to surround the PA circuits. The size of the transistors was determined by considering the required output power and gain, which was set to be 256 µm.

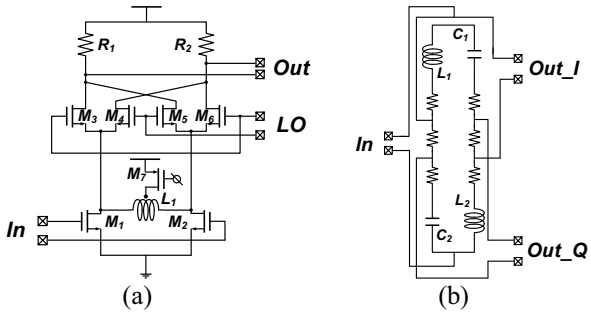


Fig. 5. Schematic of (a) the mixer and (b) the IQ generator

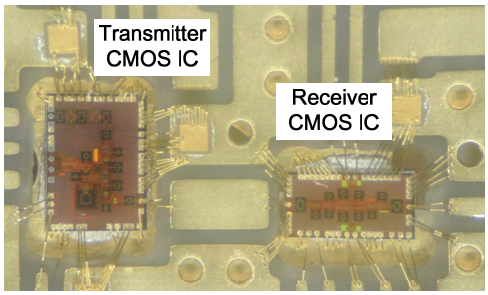


Fig. 6. The proposed transmitter and receiver CMOS ICs mounted on the module

B. Receiver (Rx)

The receiver consists of a low noise amplifier (LNA), a mixer, an IQ generator, and an additional buffer. Fig. 4 presents the circuit schematic of the LNA. To reduce the noise degradation caused by ground bouncing noise, the LNA has a differential configuration. The LNA comprises two cascode stages. The second stage employs gain control blocks to enhance the linearity of the receiver.

Both the I-mixer and Q-mixer adopt a double balanced Gilbert cell structure to suppress the even-order distortion products as shown in Fig. 5 (a). With the current-bleeding circuit, the 1/f noise is reduced and the voltage headroom problem is mitigated [5].

A quadrature all-pass filter is used to generate quadrature phase outputs as shown in Fig. 5 (b). A balanced second-order all-pass configuration offers high bandwidth and immunity to loading effects [6]. To provide a sufficiently large voltage swing at the LO ports of the I/Q mixers, additional buffers were used.

IV. Measurement Results

Fig. 6 shows a photo of the realized transmitter and receiver chips mounted on the module. Since the smaller

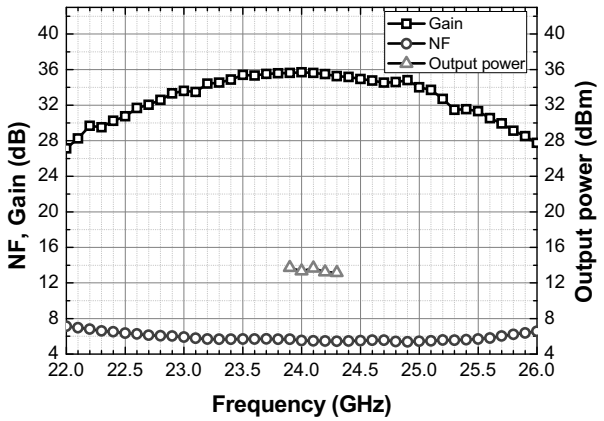


Fig. 7. Measured noise figure and gain of the receiver and output power of the transmitter

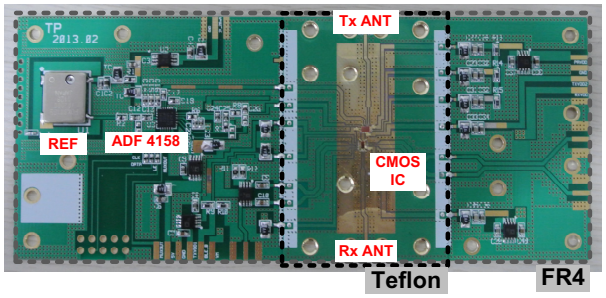


Fig. 8. The proposed FMCW radar module

bonding inductance provides wider matching networks with stable biases, the chip was mounted in a 254 µm deep cavity to minimize the length of the bond-wires. The circuit was fabricated in a 0.13-µm 1P8M RF CMOS process. The total areas of the transmitter and receiver ICs, including the pads and ESD circuits, are 1.9 mm × 1.4 mm and 1.8 mm × 0.9 mm, respectively.

The measured conversion gain and noise figure of the receiver and the output power of the transmitter versus the RF frequency are presented in Fig. 7. The receiver circuits achieve a conversion gain of 35.7 dB and a DSB noise figure of 5.5 dB at 24 GHz. The transmitter circuit obtains an output power of 13.3 dBm at 24 GHz.

The fabricated FMCW radar module is shown in Fig. 8. The module is implemented using an FR4 and Teflon substrate. A Teflon substrate is required to handle high frequency signal. The low-frequency and DC signals are handled separately on the FR4 substrate. Teflon and FR4 are connected simply by soldering without external connectors. Teflon substrate occupies only the small part of the whole module.

To connect with an antenna or measurement set-ups, the effects of the bonding inductance were compensated by simply altering the characteristic impedance of an interconnecting transmission line without stub as shown in Fig. 9 (a). The matching networks can be simplified

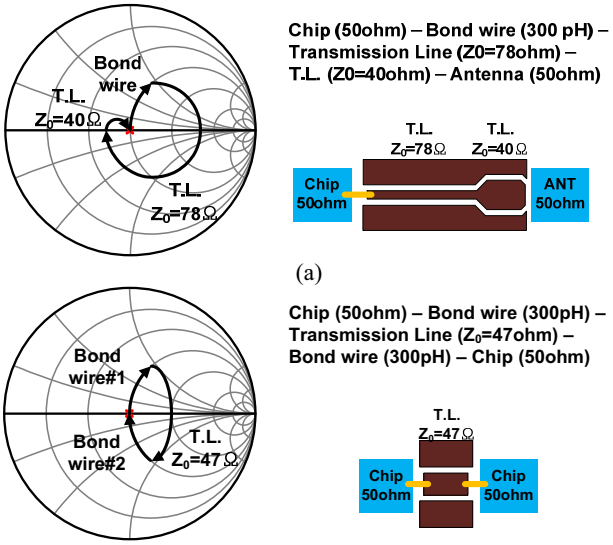


Fig. 9. The bond wire compensation networks for (a) LNA input and PA output (b) LO connection

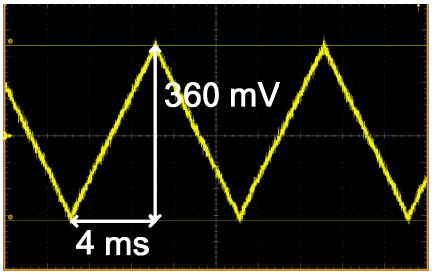


Fig. 10. The control voltage of VCO for linear frequency modulation

further in the case that both ends are connected to chip pads like the inter-connection between LO ports of the transmitter and receiver as shown in Fig. 9 (b). The bonding inductance is estimated to be 300 pH by 3D simulation HFSS.

In Fig. 10, the control voltage waveform of the VCO is shown for the linear frequency modulation with the triangular waveform, which was swept from 24 to 24.24 GHz during 4 ms. The modulation bandwidth of 240 MHz was obtained from 360 mV peak-to-peak variations of the control voltage.

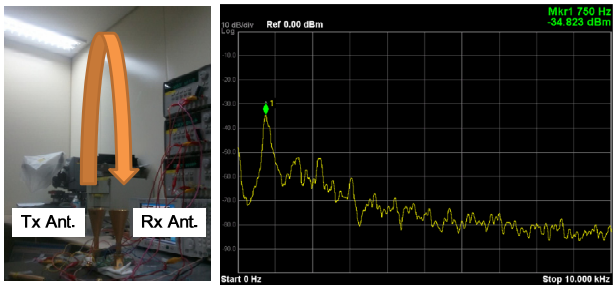
The radar module measures the distance between the ceiling of the experimental room and an antenna. Fig. 11 (a) and (b) show the measurement set-up and the output spectrum of the receiver, respectively. The extracted range from the beat frequency is 1.875 m, which agrees with that of the other reference measurement.

The performance of the FMCW radar front-end chipset is summarized and compared with the performance of previously reported radar modules in Table I. The radar chipset features a high integration level, high output power, and low noise figure, thereby achieving high

TABLE I
PERFORMANCE SUMMARY AND COMPARISONS WITH PREVIOUS WORKS

	This work	[1]	[2]	[3]
Process	130 nm CMOS	130 nm CMOS	130 nm CMOS	180 nm SiGe
Integration	I/Q Rx, VCO, PA, Divider	Rx, PA	Rx, VCO, PA, PLL	IQ Rx, VCO, PLL PA, DAC
Rx gain	35.7 dB	17 dB	19 dB	18 dB
Rx NF	5.5 dB	5.8 dB	5.4 dB*	10 dB
Rx P1dB	-31.6 dBm	-	-27 dBm	-15 dBm
Tx Phase noise	-104 dBc/Hz @ 1MHz	-	-90 dBc/Hz @ 1MHz	-102 dBc/Hz @ 1MHz
Tx output power	13.3 dBm	7 dBm	9 dBm	7 dBm
Power consumption	495 mW	42 mW	142 mW	963 mW
Chip size	Tx:1.9×1.4mm^2 Rx:1.8×0.9mm^2	2mm^2 (QFN)	0.7mm^2	5×5mm^2 (QFN)
Radar operation	O	O	X	X

*measured in separately implemented LNA chip



(a) (b)

Fig. 11. (a) Measurement set up of FMCW radar module (b) IF spectrum of receiver output

sensitivity of the radar module. The module is implemented using the proposed CMOS chipset. The FMCW radar operation is confirmed by distance measurement.

V. CONCLUSION

We presented K-band FMCW radar front-end ICs with the output power of 13.3 dBm, which are integrated in 0.13-μm CMOS technology. A high output power and low noise figure are necessary to achieve accurate long-range measurements. High output power was achieved by integrating a PA into the transmitter chip. To protect the injection locking blocks from the leakage of the PA, a fully differential topology and ground shielding were adopted. The noise figure performance was not affected by the leakage by separating two chips. As a result, we achieved the output power of 13.3 dBm and the noise figure of 5.5 dB. We implemented the FMCW transceiver module and verified the radar operation by measuring the distance of an object. This is the highest output power K-band FMCW module with CMOS front-end ICs to date.

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REFERENCES

[1] A. Hamidian, R. Ebelt, D. Shmakov, and M. Vossiek, “24 GHz CMOS transceiver with novel T/R switching concept for indoor localization,” *IEEE RFIC*, pp. 293–296, June 2013.

[2] Kim, S.-K., Cui, C., Kim, B.-S., Kim, S.Y., “A fully-integrated low power K-band radar transceiver in 130nm CMOS technology,” *Journal of Semiconductor Technology and Science*, vol. 12, no. 4, pp. 426–432, Dec. 2012.

[3] D. Saunders, et al., “A single-chip 24 GHz SiGe BiCMOS transceiver for FMCW automotive radars,” *IEEE RFIC Symp. Dig.*, Jun.2009, pp. 459–462.

[4] J. Yang, C. Kim, D. Kim, and S. Hong, “Design of a 24 GHz CMOS VCO with an asymmetric-width transformer,” *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 57, no. 3, pp. 173–177, Mar. 2010.

[5] S. -G. Lee, et al, “Current-reuse bleeding mixer”, *Electronics Letters*, Vol.36, No 8, April.2000.

[6] K.-J. Koh and G. M. Rebeiz, "0. 13-μm CMOS phase shifters for X-, Ku, and K-Band phased arrays," *IEEE J. Solid-State Circuits*, vol. 42, no. 11, pp. 2535-2546, Nov. 2007.