Implementation of Efficient Architecture of Two-Dimensional Discrete Wavelet Transform

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Abstract—This paper presents a new architecture of 2-dimensional discrete wavelet transform for JPEG2000, and the architecture is verified by implementing on FPGA board. The tile-based processing is proposed which removes the transpose buffer effectively.

Keywords—Discrete Wavelet Transform, JPEG2000

I. INTRODUCTION

Since the emergence of the JPEG2000 image compression standard [1], considerable attention has been paid to the development of efficient system architectures for the two-dimensional discrete wavelet transform (2D DWT). As the DWT is basically frame-based, large memories are required to process 2D DWT.

Basically, 2D DWT is realized by applying 1D DWT two times, column-wise and row-wise processing. In this case, the column-wise processor of the 1D DWT (CP) generates two transformed outputs, a low-pass filter output and high-pass filter output. Moving all the low-pass filter outputs toward the top side and all the high-pass filter outputs toward the bottom side makes an image being divided into L and H subband. The row-wise processor of the 1D DWT (RP) processes the outputs of the CP to generate L and H subband to be placed at the left and right side. Therefore, the CP needs a memory called the transpose buffer to save its results. For multilevel decomposition, a memory called a repeat buffer holds the previous level of LL subband, and 2D DWT repeats processing the subband.

According to the evaluation in [2], the power consumption of memory occupies a lot of portion (up to 80%) of total power dissipation. Since the size of the transpose buffer is \(O(N^2)\) when straightly implemented, we propose the tile-based processing to reduce the buffer size tremendously. The tile-based processing is proposed [6], which renders the image being segmented into a set of rectangular tiles each size of which is 2-by-2 pixels as shown in Fig. 2. Since the pre-calculation-based DWT needs a pair of the even-odd order, the tile is easily separated from the image. For each tile, the two CPs perform for each partial column, and then the two RPs start processing for each partial row data resulting from the CPs in Fig. 3. As the CPs manipulate a tile for one cycle, and the results are reordered by twisted wiring, the middle buffer is effectively removed.

The size of each temporal buffer is half than the conventional size of the temporal buffer, but the total size of the temporal buffer is the same as the conventional temporal buffer.

II. PROPOSED DWT ARCHITECTURE

The size of the transpose buffer in the conventional 2D DWT architecture is \(O(N^2)\) when straightly implemented, we propose the tile-based processing to reduce the buffer size tremendously. The tile-based processing is proposed [6], which renders the image being segmented into a set of rectangular tiles each size of which is 2-by-2 pixels as shown in Fig. 2. Since the pre-calculation-based DWT needs a pair of the even-odd order, the tile is easily separated from the image. For each tile, the two CPs perform for each partial column, and then the two RPs start processing for each partial row data resulting from the CPs in Fig. 3. As the CPs manipulate a tile for one cycle, and the results are reordered by twisted wiring, the middle buffer is effectively removed.

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III. COMPARISON AND VERIFICATION

A. Comparison

Most architectures of 2D DWT requires large memory, many research have been optimized the memory usages. In the architecture, there is a transpose buffer changing the scanning direction between RP and CP. Moreover, as most architectures processes in raster format, temporal buffer is required for holding intermediate values of CP. Several researches of the architectures of 2D DWT are compared with the proposed on Table I. Barua et al. [4] propose a hybrid of level-by-level and line-based architectures for 2D DWT, in which the image is scanned into the RP in raster format. A large buffer whose role is similar to that of the transpose and temporal buffer is located between RP and CP, and \(7N\) is larger than the proposed. Huang et al. [3] optimize the size of transpose buffer based on the different speed of filling and being consumed, and Wu et al. [5] also adopt the idea. However, since the size of transpose buffer is dependent on the 1D size of the input image, it has to be reduced further. The proposed architecture adopts the tile processing, so that the transpose buffer effectively removes.

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B. Verification

The proposed 2D DWT is verified by implementation on FPGA board (Terasic DE2). The system is integrated on the FPGA, which includes the proposed 2D DWT processor, RISC processor, program and data memory, and LCD controller as shown in Fig. 5. The RISC processor segments an image into 64-by-64 pixel blocks only for verification, and each block is processed by the proposed 2D DWT. After finishing 2D DWT processing, RISC processor transfers each block result of 2D DWT attaching the original block on the lowest level of HL, LH and HH subbands, and LCD controller display the results as shown in Fig. 6.

IV. Conclusion

The tile-based processing for 2D DWT removes the transpose buffer effectively, and is well verified on FPGA board. Since the size of the repeat buffer is also large, reducing the size of the buffer will be researched.

REFERENCES