Low-Power and High-Accurate Synchronization for IEEE 802.16d Systems

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Abstract—Orthogonal frequency division multiplexing (OFDM) is a viable technology for high-speed data transmission by virtue of its spectral efficiency and robustness to multi-path fading. These advantages can be achieved only with good synchronization both in time and frequency. This paper proposes new efficient synchronization methods for an OFDM-based system, IEEE 802.16d. For the coarse time synchronization and the fractional carrier frequency offset (CFO) estimation, a disjoint architecture is proposed that performs auto-correlations separately to achieve more reliable frequency synchronization and to reduce overall hardware complexity and power consumption. In addition, for the fine symbol timing offset (STO) and the integer CFO, a new joint estimation method employing parallel cross-correlations between the received samples and the pre-rotated training sequences is proposed. Experimental results show significantly superior performance to the previous synchronization methods. A prototype synchronizer based on the proposed methods is designed with a 0.25-μm CMOS process, which reduces power consumption by more than 60% compared to a conventional synchronizer.

Index Terms—Carrier frequency offset (CFO) estimation, IEEE 802.16d, orthogonal frequency division multiplexing (OFDM), symbol timing offset (STO) estimation, synchronization, WiMAX.

I. INTRODUCTION

IEEE 802.16d, known as fixed WiMAX, is a promising technology for wireless MAN due to its high data transmission rate and scalability [1]. It is based on the orthogonal frequency division multiplexing (OFDM) in which the data distributed on a number of orthogonal sub-channels are modulated by using the discrete Fourier transform [2], [3]. The OFDM presents an effective solution for the frequency selectivity mainly caused by the multi-path fading, and mitigates the inter-symbol interference by allocating a relatively low data rate to each sub-channel and providing the cyclic prefix (CP) of the symbol.

As sub-channel bands are overlapping one another to achieve a fairly good spectral efficiency in OFDM systems, the performance is very sensitive to the sub-channel interference that is mainly caused by the frequency offset [4]. Additionally, the timing offset larger than the cyclic prefix leads to the inter-symbol interference, degrading the system performance severely. Therefore, the advantages of OFDM systems can be achieved only with good synchronizations both in time and frequency.

A general synchronization scheme widely used in burst-mode OFDM systems such as IEEE 802.16d is to calculate the auto-correlation of the received samples [5]–[11]. As the scheme is robust to noise and carrier frequency offset (CFO), it is attractive for the time synchronization of noisy samples. In addition to this, the CFO can be jointly estimated in the scheme. However, the accuracy of the time synchronization is low and the estimation range of the CFO is limited. Since the scheme is insufficient for meeting the tight synchronization demanded for such systems as IEEE 802.16d, it is required to estimate the fine symbol timing offset (STO) and the integer CFO being out of the estimation range [8].

The synchronization has significant effects on the overall performance of the receiver. A failure of the coarse time synchronization leads to the missing or false alarming of a preamble, making all of the rest steps meaningless. If the CFO and the fine STO are not corrected properly, they cause interference between sub-channels and symbols. In addition, it may take a time as long as 2 MAC frames to search for a preamble in IEEE 802.16d systems [1]. During the searching time, the coarse time synchronization unit should be active, whereas all the other units can be deactivated to save energy. The power efficiency of the synchronization unit is therefore significantly important in achieving low power receivers.

This paper deals with all aspects of the synchronizations required in IEEE 802.16d systems. For the coarse time synchronization and the fractional CFO estimation, a disjoint architecture is proposed that performs auto-correlations separately to achieve more reliable frequency synchronization and to reduce overall hardware complexity and power consumption. We also propose a new method to jointly estimate the fine STO and the integer CFO. The proposed method is to perform parallel cross-correlations between the received samples and the pre-rotated training sequences. In addition, an on-the-fly computation scheme is proposed to reduce the overall processing latency without employing additional buffers.

The rest of this paper is organized as follows. In Section II, the previous synchronization methods are analyzed along with their merits and demerits, and the overall procedure of the proposed synchronizations is described. Section III describes the new architecture for the coarse time synchronization and the fractional CFO estimation, and Section IV proposes the joint estimation scheme for the fine STO and the integer CFO. Section V discusses performance and implementation results of the proposed synchronizer.
II. PREVIOUS WORKS FOR SYNCHRONIZATIONS

This section summarizes the conventional synchronization algorithms applied to burst-mode OFDM systems, focusing on their merits and drawbacks, and presents an overall procedure of the proposed synchronizations.

A. Coarse Time Synchronization and CFO Estimation

The autocorrelation between the received samples is commonly adopted for these synchronizations. As shown in Fig. 1, the downlink preamble of IEEE 802.16d consists of four short training sequences and two long training sequences, each of which follows a cyclic prefix of the corresponding training sequence. The main objective of the repetitive short training sequences is to detect the preamble by performing auto-correlation [1], and the long training sequences are usually used to estimate the fading factors of the channels. To make the auto-correlation independent of the channel environment, the normalized auto-correlation defined below is usually employed [5]–[10]

$$\rho_n = \frac{1}{W} \sum_{i=1}^{W} r_{n-i} \cdot r_{n-i-W}^* \left/ \left( \sum_{i=1}^{W} |r_{n-i}|^2 \right) \right.$$  \hspace{1cm} (1)

where $r_n$ is the $n$th received sample and $W$ denotes the length of the short training sequence, 64 for the downlink preamble of IEEE 802.16d. The auto-correlation between the repetitive training sequences makes $\rho_n$ prominently high in the time domain, forming a magnitude plateau as shown in Fig. 2. The receiver searches for the preamble so as to detect the preamble, which is achieved in practice by comparing the magnitude of the auto-correlation to a threshold. In addition, $\rho_n$ can also be used to estimate the CFO as the phase difference between $r_{n-i}$ and $r_{n-i-W}$ is constant and proportional to $W$ if the CFO is assumed to be time-invariant.

As this joint estimation based on the auto-correlation is attractive because of its simplicity and robustness, most of the previous architectures use a unified auto-correlator to obtain both of the time synchronization and the CFO estimation jointly at the same time [5]–[9]. However, there are some drawbacks to be improved. First, the previous architectures do not seriously take into account the samples involved in the auto-correlation, leading to a significant performance degradation of the CFO estimation. The plateau boundary is usually detected by comparing the auto-correlation with a threshold in the previous works, and the auto-correlation is used to estimate the CFO at the same time. Let us assume that the auto-correlation magnitude becomes greater than the threshold as the received samples are serially fed into the unified auto-correlator. In this case, that point may be near the plateau but not exactly in the plateau. Examining the estimation window involved in the auto-correlation, we often find that some of the samples in the window are out of the short training sequences, as indicated in the left CFO estimation window in Fig. 2. This can occur even if the timing is achieved by detecting the falling edge of the auto-correlation as depicted in the right CFO estimation window in Fig. 2. Only within the plateau, we can guarantee that the estimation window is in the short training sequences. As the CFO is estimated based on the phase difference between the repetitive training sequences, the CFO estimation can be degraded by the incorrect samples in the estimation window, if estimated jointly with the plateau detection. Some works have revised this problem by detecting a peak instead of the threshold comparison or by employing other metrics, but such an approach increases the complexity considerably [7]. Second, maintaining the same precision in the two estimations may be wasteful. In general, the time synchronization requires much less precision than the CFO estimation does. The coarse time synchronization can be successful even with a reduced hardware unit exploiting this property [20].

There have been some schemes employing cross-correlation [13] for the coarse time synchronization. Although such a scheme achieves fairly good accuracy even in a low signal-to-noise ratio (SNR), it can be applied only to the time synchronization, not to the CFO estimation. Moreover, the cross-correlation is very sensitive to the CFO, making the time synchronization unreliable if there is a small CFO. In general, this scheme is appropriate for the fine STO estimation that deals with CFO-corrected samples.

B. Fine STO Estimation

The objective of the fine STO estimation is to detect the starting point of a discrete Fourier transform (DFT) window, which is needed for the OFDM demodulation in the receiver. As two long sequences in the downlink preamble are usually demodulated to estimate the fading factors of the channels [1], the fine STO estimation should be completed prior to the long training sequences.

A simple scheme to estimate the fine STO is to detect the last boundary of the short training sequences, as the boundary is the starting point of the long training sequences. It can be achieved by perceiving the falling edge of the auto-correlation curve [6]. This scheme is robust to the CFO and leads to a simple hardware implementation. As the coarse time synchronization is usually based on the auto-correlation, a hardware structure similar to that used for the coarse time synchronization can be applied...
here. Besides, it is not complex if the incremental auto-correlation form that can be implemented with only two complex multipliers and an accumulator is employed [5]. However, it is almost impossible to apply this scheme to the systems requiring high estimation accuracy. In IEEE 802.16d, for example, the allowed STO ranges from $-4$ samples to $+4$ samples, which is too tight for this scheme to meet.

To achieve more accurate estimation, the cross-correlation between the received samples and the training sequences have been performed [8], [10], [13], [16]. When they are matched together, the cross-correlation has a peak. We can estimate the boundary of the short training sequences by detecting the peak. This scheme can achieve high estimation accuracy and can be successful in a very low SNR. Additionally, if negligible performance degradation is allowed in the peak detection, the cross-correlation can be performed with a very small bit-width [16], which enables $W$ complex multiplications and their summation to be calculated in a clock period affordable in practical implementation. This scheme is, however, much vulnerable to the CFO. If this scheme is applied to the samples contaminated by some CFO, it can result in severe performance degradation, as the peak is no longer prominent.

**C. Integer CFO Estimation**

To represent the interfering effect, the CFO is usually normalized by the sub-carrier spacing. The integer part of the normalized CFO represents a cyclic shift in the frequency domain symbol, while the fractional part causes the interference between sub-channels. For the latter, the average phase difference between two samples corresponding to the same position in the training sequence is measured by performing the auto-correlation. However, the estimation range is limited. In IEEE 802.16d, for instance, its range is up to $\pm 2$ sub-carrier spacings, whereas the CFO can be larger than this range.

The integer CFO is commonly estimated in the frequency domain by performing cross-correlation [8], [12], [14]. As this offset causes a cyclic shift in the frequency domain, the cross-correlation between the training sequence and the cyclic shifted symbol is performed in the frequency domain. This can be expressed as follows:

$$\arg\max_{d} \left[ \sum_{k=1}^{N} S_k^{*} R_{k}(k+d)\%N \right]$$

where $R_k$ and $S_k$ are the $k$th frequency components of the received symbol and the training sequence, respectively. The symbol size $N$ is equal to the DFT size, and the modulo operation is represented by $\%$. The integer CFO is estimated by searching for a shift amount that yields a peak in the cross-correlation as expressed in (2). The shift amount $d$ is usually a multiple of the estimation range of the fractional CFO, because only the integer CFO remains once the fractional CFO is corrected [8]. Though this scheme is intuitive, it needs almost perfect time synchronization to achieve a reasonable performance [14]. To work-around this problem, the cross-correlation is modified with the concept of the coherence phase bandwidth so as to estimate the integer CFO even in the case of moderate symbol timing offset [14]. Moreover, the integer CFO estimation should be performed before the channel estimation. To acquire the channel information, the long training sequences in the preamble are usually used especially in burst-mode OFDM systems such as IEEE 802.16d [1]. Thus, the integer CFO estimation should be performed in an early processing stage.

**D. Overall Synchronization Procedure**

The overall procedure of the proposed synchronization is depicted in Fig. 3, which works according to the following three steps:

1) coarse time synchronization using auto-correlation;
2) fractional CFO estimation using precise auto-correlation;
3) fine STO and integer CFO estimation.

The coarse time synchronization is to detect the starting point of a frame. For this, the received samples are quantized to a few bits in order to reduce computational complexity and then the normalized auto-correlation performed for the quantized samples is compared to a threshold. The fractional CFO is estimated by performing more precise auto-correlation only for $W$ samples coming after the coarse time synchronization, where $W$ is 64 samples long in IEEE 802.16d. Both of these synchronizations are based on auto-correlation, but the auto-correlation accuracy desired for the coarse time synchronization is dissimilar to that for the fractional CFO estimation. Instead of the unified auto-correlator employed in the previous joint approach, therefore, a disjoint auto-correlator is used for each synchronization to optimize it separately with considering its desired accuracy. Using the CORDIC-like processing proposed in [17], we correct the fractional CFO of the following samples. To determine the boundary of the short training sequences, the samples whose fractional CFO is corrected are involved in the fine STO estimation that performs cross-correlation for $2W$ samples. The integer CFO is estimated jointly with the fine STO estimation in the time domain.

**III. DISJOINT ARCHITECTURE FOR COARSE TIME SYNCHRONIZATION AND FRACTIONAL CFO ESTIMATION**

In the previous architectures, the coarse time synchronization and the CFO estimation are jointly performed based on a unified auto-correlator [6]–[10]. This approach is inefficient as the precisions required in the two auto-correlations differ from each other. Through a number of the fixed-point simulations, it turns out that the bit-width for the fractional CFO estimation should...
be about 10 bits to obtain a reasonable performance [10], [11] while the coarse time synchronization requires only 4 bits as shown in Fig. 4. According to this observation, the proposed architecture has two separate parts to optimize them individually, as shown in Fig. 5. The lower part is for the coarse time synchronization, and the upper part is for the precise auto-correlation to be used for the fractional CFO estimation. These are expressed as follows, respectively

\[
\mu_n = \left[ \sum_{i=1}^{W} r_{n-i} \cdot r_{n-i-W}^{*} \right] / \left( \sum_{i=1}^{W} |r_{n-i}|^2 \right) ^{2} \tag{3}
\]

\[
\Lambda_n = \sum_{i=1}^{W} r_{n-i} \cdot r_{n-i-W}^{*} \cdot \tag{4}
\]

Both of them calculate the auto-correlations, but their bit-widths are different. In other words, \( r_n \) in (3) is represented in a smaller bit-width than \( r_n \) in (4).

**A. Auto-Correlator for Coarse Time Synchronization**

To derive a more efficient computational structure, the auto-correlation is transformed to an incremental form [5] as follows:

\[
\Lambda_n = \sum_{i=1}^{W} r_{n-i} \cdot r_{n-i-W}^{*} = \Lambda_{n-1} + r_{n} \cdot r_{n-W}^{*} - r_{n-W} \cdot r_{n-2W}^{*} \tag{5}
\]

The incremental auto-correlation requires \( 2W \) sample buffers whose length is equal to 128 for the short training sequences of the downlink preamble [1]. In the proposed architecture, the sample buffers are implemented as circular buffers, as shown in Fig. 5. In the coarse time synchronization, \( \mu_n \) is compared to a threshold, which can be efficiently implemented with no division as follows:

\[
\left\| \sum_{i=1}^{W} r_{n-i} \cdot r_{n-i-W}^{*} \right\|^2 - Th \cdot \left( \sum_{i=1}^{W} |r_{n-i}|^2 \right) > 0 \tag{6}
\]

where \( Th \) means the threshold. If the threshold is a power of two, the multiplication in the second term can be replaced by a shift operation. Through a number of simulations, the threshold is determined to 1/4. As stated before, the coarse time synchronization can be successful even if the samples are represented in a small bit-width, leading to low power consumption and less complexity in hardware design.

As depicted in Fig. 6(a), the incremental auto-correlation expressed in (5) may be implemented in a straightforward way. In the figure, we can find that a pair of two multiplications has a common operand such as \( \text{Re}(r_{n-W}) \), \( \text{Im}(r_{n-W}) \), \( \text{Re}(r_{n-W}) \), or \( \text{Im}(r_{n-W}) \). The other operands can be added before the multiplication to reduce the number of multipliers, which enables eight multiplications to be implemented with four multipliers as shown in Fig. 6(b). Additionally, the carry save addition is employed to add three operands in a more economical way.

**B. Adaptive Selection of Dual Auto-Correlators for Coarse Time Synchronization**

The coarse time synchronization is improved to further reduce power consumption. As shown in Fig. 4, considering only
In Fig. 7, where there are three states. Two states use coarse time synchronization based on the finite-state machine concurrently with the precise auto-correlation for the sign-quantized samples coming after the coarse time synchronization, if the SNR is not low. To exploit this fact, a small hard-ware unit that performs one-bit auto-correlation for the sign-quantized samples is enough for the coarse time synchronization, if the SNR is not low.

According to the current SNR that is approximately determined by the following equations, one of the two auto-correlators is selected adaptively for the coarse time synchronization:

\[
\sum_{i=1}^{W} r_{n-i}^* \cdot r_{n-i-W} = \sum_{i=1}^{W} (x_{n-i} + w_{n-i})^* \cdot (x_{n-i-W} + w_{n-i-W}) \\
\approx W \cdot \sigma_x^2
\]  

(7)

\[
\sum_{i=1}^{W} r_{n-i}^* \cdot r_{n-i} = \sum_{i=1}^{W} (x_{n-i} + w_{n-i})^* \cdot (x_{n-i} + w_{n-i}) \\
\approx W \cdot \sigma_x^2 + W \cdot \sigma_w^2
\]  

(8)

\[
\left( \frac{\sum_{i=1}^{W} r_{n-i}^* \cdot r_{n-i-W}}{\sum_{i=1}^{W} r_{n-i}^* \cdot r_{n-i} - \sum_{i=1}^{W} r_{n-i}^* \cdot r_{n-i-W}} \right) \approx \text{SNR}
\]  

(9)

where \(x_n\) and \(w_n\) are the \(n\)th samples of the channel response of the transmitted signal and the additive zero-mean noise which is statistically uncorrelated, respectively. As the signal energy \(\sigma_x^2\) and the noise energy \(\sigma_w^2\) are approximated as (7) and (8), the SNR can be estimated as (9).

Note that the SNR is estimated with the sign-quantized samples, and the sign-quantization can be achieved by taking the most significant bit in the 2’s complement representation. The SNR estimation does not need to be accurate but should be enough to decide whether the current SNR is high or low. Given a threshold, \(T_{\text{SNR}}\), the decision can be made with no division as follows:

\[
\left( \frac{\sum_{i=1}^{W} r_{n-i}^* \cdot r_{n-i} - \sum_{i=1}^{W} r_{n-i}^* \cdot r_{n-i-W}}{\sum_{i=1}^{W} r_{n-i}^* \cdot r_{n-i-W}} \right) > 0. \]  

(10)

The hardware complexity is low enough to be negligible. If a high SNR is incorrectly decided to be low, it does not degrade the synchronization performance. Thus, a pessimistic decision is preferable. This SNR decision can be performed for the \(W\) sign-quantized samples coming after the coarse time synchronization, concurrently with the precise auto-correlation for the fractional CFO estimation.

One of the two auto-correlators is adaptively selected for the coarse time synchronization based on the finite-state machine shown in Fig. 7, where there are three states. Two states use the four-bit auto-correlator and one state uses the one-bit auto-correlator. Since the channel does not change abruptly in the target system, the conservative state transitions are desirable.

In State1, two successive decisions of high SNR are needed to transit to State2, where the one-bit auto-correlator is used for low power consumption. Even if the current SNR is falsely decided to be high one time, such a one-time false decision does not degrade the performance because two successive false decisions are needed to actually change to State2. However, only one state exists for high SNR, as the false decision in State3 does not degrade the performance.

If the SNR is decided to be high, only the simple one-bit auto-correlator is used and the other one whose bit-width is...
relatively large is not activated to achieve lower power consumption. Otherwise, the larger auto-correlator is solely activated. Since the coarse time synchronization is active up to 2 MAC frames [1], the simple auto-correlator lowers the dynamic power consumption by reducing switching activity in a high SNR. As the coarse time synchronization unit is solely active for the long time, this improvement has a significant meaning. The one-bit auto-correlator can be expressed as (5), except that is a sign-quantized sample. The multiplication with the sign-quantized samples can be implemented with a few gates. In addition to this, as the products of the sign-quantized samples can be either or , the energy calculated for the sign-quantized samples is constant, meaning that we can eliminate the energy calculation.

C. Auto-Correlator for Fractional CFO Estimation

Since only the average phase difference is needed for the fractional CFO estimation, the auto-correlation does not need to be normalized. Therefore, the hardware resources calculating energy are eliminated as shown in Fig. 5. Moreover, the auto-correlation is calculated only once for samples after the coarse time synchronization is completed. It can be calculated with a complex multiplier and an accumulator more efficiently than the incremental form that needs two complex multipliers, as shown in Fig. 8. Though the incremental form is effective in computing many auto-correlations for a sequence of symbols, it is not needed in the proposed architecture, as the fractional CFO estimation deals with only samples coming after the coarse time synchronization.

In addition, the disjointed auto-correlations have an advantage that the fractional CFO estimation is more accurate than the previous joint estimation. In the proposed architecture, the phase difference of the samples coming after the coarse time synchronization are considered for the fractional CFO estimation, whereas the previous architectures usually estimate the fractional CFO based on the auto-correlation calculated at the moment when the preamble is detected by comparing to a threshold [5]–[9]. This can cause a negative effect on the estimation performance because some incorrect samples can be included in the estimation window as explained in Section III-A. As shown in Fig. 9, W samples considered in the proposed architecture are guaranteed to be within the short training sequences, because they are taken after the coarse time synchronization is done. Therefore, we can expect that the accuracy of the fractional CFO estimation is significantly improved due to the purity of the samples involved in the precise auto-correlation.

IV. JOINT ESTIMATION OF FINE STO AND INTEGER CFO

A new method that can jointly estimate the fine STO and the integer CFO in the time domain is proposed in this section. The proposed method is based on the parallel cross-correlations with the pre-rotated sequences, and is free from the dependence problem that one estimation has a significant impact on the following estimation. Additionally, since both estimation results are available at the same time, no extra buffers are required for the integer CFO estimation.

A. Analysis of Integer CFO

The fractional CFO can be corrected before the fine STO estimation by computing the auto-correlation as described in the previous section [8]. As the received samples are rotated in proportion to the CFO, they can be represented by the phasor as shown in Fig. 10(a), where the received samples, , and have complex values. Since the two samples correspond to the same position of the training sequence, they were originally equal to each other. The rotation of is expressed as

\[ r_n \equiv e^{j\theta} r_{n-W} \]  

(11)
where $\theta$ is the phase difference between the two samples. Based on this relation, we can estimate the CFO as $\theta / W$. This estimation is inaccurate when the rotation is more than a revolution, as shown in Fig. 10(b). In this case, $r_n$ can be represented as follows:

$$r_n = e^{j2m\pi}e^{j\theta}r_{n-W}$$  \hspace{1cm} (12)

where $m$ is the number of revolutions. We recognize the phase difference $\theta$ in the range of $[0, 2\pi)$, while the actual CFO is

$$\frac{2m\pi + \theta}{W} = \frac{2m\pi}{W} + \frac{\theta}{W}.$$  \hspace{1cm} (13)

In this case, the CFO is estimated as $\theta / W$ although the actual CFO is $(2m\pi + \theta)/W$. Therefore, the residual CFO $(2m\pi / W)$ remains in the samples even after the CFO is corrected. The rotation due to this residual component is represented as

$$e^{j2m\pi/W} = \omega_N^{-m} = \omega_N^{-km}$$  \hspace{1cm} (14)

where $N$ which is expressed as $W$ times $k$ is the number of the DFT points and $\omega_N$ is the unit twiddle factor $\exp(-j2\pi/N)$. As $N = 256$ and $W = 64$ or 128 in the target system [1], $k$ is either 4 or 2, respectively. In (14), the remaining term is an integer multiple of the sub-carrier spacing, and can be regarded as an integer power of the unit twiddle factor. The integer CFO causes a cyclic shift of the symbol in the frequency domain as indicated by the shifting property of DFT. Fig. 11 illustrates the integer CFO remaining in the received samples, where a CFO of +5.5 sub-carrier spacings is exemplified with assuming that the fractional CFO range estimated by the short training sequence is -2 to +2 sub-carrier spacings. If the fractional CFO is corrected in the preceeding steps, the samples to be used for the fine STO estimation have only a CFO that is an integer multiple of the estimation range of the fractional CFO. This assumption is usually valid for the synchronizer of burst-mode OFDM receivers [8].

### B. Cross-Correlation With Pre-Rotated Sequences

To exploit the discreteness of the residual integer CFO, we propose a new estimation scheme. The worst CFO specified in the profile of IEEE 802.16d is less than ±6 sub-carrier spacings [1]. Once the fractional CFO that can be estimated up to ±4 sub-carrier spacings is first corrected using the short training sequences, the residual integer CFO can be 0 or ±4 sub-carrier spacings. In other words, $k = 4$ and $m = \pm 1$ or 0 in (14). Since the integer CFO is limited to three cases, we can prepare the pre-rotated training sequences each of which is rotated by one of the possible integer CFOs. The pre-rotated training sequence can be expressed as

$$s_{n,p} = s_n \cdot \omega_N^{pm}$$  \hspace{1cm} (15)

where $p$ is 0 or ±4 and $s_n$ is the $n$th sample in the training sequence. Let $\tilde{r}_n$ be the sample of which fractional CFO is corrected. As the residual CFO of $\tilde{r}_n$ is 0 or ±4, $\tilde{r}_n$ must be matched with one of the pre-rotated sequences, $s_{n,0}$, $s_{n+4}$, and $s_{n-4}$. The matched one will have a large peak. If the peak occurs at $n_p$ then the fine STO and the integer CFO correspond to $n$ and $p$, respectively. We can formalize this observation as

$$(n_p, p) = \arg \max_{n, p} |X_{n,p}|$$  \hspace{1cm} (16)

where $X_{n,p}$ denotes the cross-correlation between $\tilde{r}_n$ and $s_{n,p}$.

For example, the proposed estimation is simulated with a CFO of ±5.5 sub-carrier spacings in a multi-path fading environment in which the channel parameters conform to those of the SUI-3 channel and the SNR is 2 dB [15]. As shown in Fig. 12, where $X_{n,p}$ is plotted separately for each $p$, the peak occurs at $n = +25$ and $p = -4$, implying that the fine STO is +25 and the integer CFO is ±4 sub-carrier spacings. Note that the fine STO and the integer CFO are jointly estimated in the time domain, while the integer CFO is conventionally estimated in the frequency domain.

Fig. 13 shows the hardware architecture for the proposed scheme. This architecture can be thought as a combination of three 64-tap FIR filters. The filter coefficient of each tap is hard-
wired for a pre-rotated sequence expressed in (15). The direct form is suitable for the hardware implementation because the total number of buffers is less than that of the transposed form and the cross-correlation does not need to operate at a high clock frequency.

It is important to reduce the complexity of the 2-D search in (16). First of all, the 2-D search is converted to two 1-D searches. For each sample, three cross-correlations are calculated, but only one that is associated with the maximal value is considered as a candidate for the peak. Then the peak is chosen among the candidates. As depicted in Fig. 13, this structure is simple and easy to implement. Second, the cross-correlation can be calculated with the sign-quantized samples as shown in Fig. 13, as it is sufficient to detect the peak relatively rather than absolutely. At the cost of a little performance degradation, moreover, the absolute operation can be approximated as the following equation:

\[ |x + jy| \approx |x| + |y| \]  

(17)

where \(x\) and \(y\) are real numbers. Finally, since the joint estimation is active for a very short time as indicated in Fig. 3, the power increased by the parallel processing has a negligible effect on the overall power consumption of the target system.

V. EVALUATIONS

The performance of the proposed synchronization is evaluated through a number of simulations performed with a multi-path fading channel whose parameters are conformed to the SUI-3 channel for all the SNR range specified in IEEE 802.16d [1], [15].

A. Performance of Coarse Time Synchronization and Fractional CFO Estimation

Fig. 14 compares the performance of the coarse time synchronization. The received samples are quantized to either four bits or one bit according to the SNR, while they are represented with more bits in the conventional unified architectures. We can see in the figure that the proposed architecture performs comparably to the previous architecture, even though the samples are represented with a much less bit-width. Additionally, the adaptive selection of the dual auto-correlators for the coarse time synchronization performs well compared to the case that the auto-correlator corresponding to high SNR is used solely.

Fig. 15, where the proposed approach performs the auto-correlation for the \(W\) samples coming after the coarse time synchronization and the conventional architecture shares the auto-correlation used for the coarse time synchronization, jointly [8]. As there is no ambiguity in selecting samples to be involved in this estimation, the proposed approach shows better performance than the previous one.

B. Performance of Joint Estimation of Fine STO and Integer CFO

Fig. 16 shows the performance of the fine STO estimation, where errors are presented in an RMS manner. The STO should be lower than 4 in the target system if the channel SNR is above 2 dB [1]. Compared to the conventional architecture, the proposed architecture shows excellent performance in the fine STO estimation for every SNR simulated and meets the performance...
Fig. 17. Performance result of the integer CFO estimation.

requirement, whereas the conventional one does not. The auto-
correlation-based architecture is used in the comparison, be-
cause this estimation should be robust to the residual integer
CFO. The architecture based on a single cross-correlation is not
appropriate because its sensitivity to the residual integer CFO is
severe.

Fig. 17 shows the simulation results of the integer CFO es-
timation, which compares the result of the proposed architec-
ture with those of the two previous ones. One performs the con-
tventional cross-correlation in the frequency domain with the
cyclic-shifted sequences, as defined in (2) [8], [12], and the other
performs the cross-correlation modified with the concept of the
coherence phase bandwidth proposed in [14]. To achieve robust-
ness to the CFO, both of the previous schemes assume that the
fine STO was accurately estimated by performing the auto-cor-
relation. Therefore, the previous estimations work well only if
the fine STO is estimated accurately prior to the integer CFO.
The performance of the proposed architecture is excellent even
in a very low SNR. Additionally, the proposed architecture can
estimate the integer CFO in the time domain jointly with the
fine STO, while the previous architectures have to estimate them
separately and cannot estimate the integer CFO until the symbol
is transformed to the frequency domain. This means that the pro-
posed architecture can reduce the overall processing latency and
the buffers required to store the samples.

C. Prototype Design

The proposed and the conventional architectures are both de-
signed with a 0.25-μm CMOS standard cell library and syn-
thesized under the same constraints. It is difficult to compare
the proposed system directly with the previous ones, because
there have been few works implementing the entire synchro-
nizer system. Most of the previous works have been concen-
trated on a single synchronization instead of whole synchroniza-
tions. Thus, we individually compare each block to the corre-
sponding conventional block.

The gate counts are compared in Table I, where a two-input
NAND cell is counted as one. The conventional one was im-
plemented based on the algorithms explained in Section II. In
Table I, the other blocks such as the controller and the memory
 glue logic are not listed for simplicity, as their hardware com-
plexities are not considerable. In terms of the total gate counts,
the proposed architecture has an overhead of 3.3%. The over-
head is a cost to be paid for the excellent synchronization perfor-
mance. Moreover, the proposed system estimates the fine STO
and the integer CFO at the same time, while the conventional
one in the table estimates only the fine STO. In the conventional
architecture, an additional hardware unit is indispensable to es-
imate the integer CFO in the frequency domain, which is not
included in the comparison.

To investigate the power efficiency of the proposed architec-
ture, the power simulation for the coarse time synchronization
and the auto-correlation of the fractional CFO estimation is per-
formed for the gate-level design annotated with switching ac-
tivities. The power consumption of the other blocks is negli-
gible because their active times are tiny. The results are shown
in Fig. 18 and Table II, where we can see that the proposed ar-
chitecture reduces the power consumption by 61% on the av-
erage compared to the conventional one. This is a natural con-
sequence, since the coarse time synchronization unit that is the
dominant source of the power consumption in the overall system
is disjointed and optimized separately. Besides, the adaptive se-
lection of the dual auto-correlators for the coarse time synchro-
nization is helpful to further reduce the power consumption. In
our simulation, the percentage of selecting the one-bit auto-cor-
TABLE II
POWER CONSUMPTION COMPARISON

<table>
<thead>
<tr>
<th>SNR (dB)</th>
<th>PROPOSED(^a) (A) (MW)</th>
<th>CONVENTIONAL (B) (MW)</th>
<th>A/B</th>
</tr>
</thead>
<tbody>
<tr>
<td>-1</td>
<td>6.127</td>
<td>15.359</td>
<td>0.399</td>
</tr>
<tr>
<td>2</td>
<td>6.211</td>
<td>14.741</td>
<td>0.421</td>
</tr>
<tr>
<td>5</td>
<td>6.027</td>
<td>15.422</td>
<td>0.391</td>
</tr>
<tr>
<td>8</td>
<td>5.438</td>
<td>16.225</td>
<td>0.335</td>
</tr>
<tr>
<td>11</td>
<td>4.817</td>
<td>15.242</td>
<td>0.316</td>
</tr>
<tr>
<td>14</td>
<td>4.863</td>
<td>15.799</td>
<td>0.308</td>
</tr>
<tr>
<td>17</td>
<td>4.795</td>
<td>16.310</td>
<td>0.294</td>
</tr>
<tr>
<td>20</td>
<td>4.828</td>
<td>16.038</td>
<td>0.301</td>
</tr>
</tbody>
</table>

\(^a\)Proposed design with the adaptive selection of the dual auto-correlators.

Fig. 19. Die photo of the proposed synchronizer.

The die photo of the proposed synchronizer fabricated on a 0.25-\(\mu\)m CMOS process is shown in Fig. 19. The chip occupies a die area of 800 \(\mu\)m \(\times\) 750 \(\mu\)m, and operates at 20 MHz.

VI. CONCLUSION

In this paper, we have proposed new synchronization architectures for IEEE 802.16d systems. For the coarse time synchronization and the fractional CFO estimation, a disjoint architecture is proposed to reduce the hardware complexity and power consumption by optimizing them individually. The fractional CFO estimation is made accurate by eliminating incorrect samples that do not correspond to the training sequences. To reduce the power consumption of the coarse time synchronization, a simple auto-correlator is used exclusively in a high SNR, which is adaptively selected by measuring the current SNR. Second, we have proposed an efficient method to jointly estimate the fine STO and the integer CFO. The proposed approach is to perform the cross-correlations between the received samples and the pre-rotated training sequence. The simulation results show that the proposed approach outperforms the previous ones in both estimations. Since the fine STO and the integer CFO are jointly estimated in an on-the-fly manner, the proposed approach requires no additional buffers. In addition, the proposed joint estimation has an effect of eliminating the dependence problem of the two estimations, whereas the dependence is inevitable in the previous approaches estimating them successively. With the proposed architectures, the tight synchronization performance required for the target system IEEE 802.16d could be met successfully. As other burst-mode OFDM systems such as IEEE 802.11a [18] and IEEE 802.11n [19] have frame structures similar to the target system, the proposed synchronization architectures can be applied to them.

REFERENCES


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