Fast Frequency Acquisition Phase Frequency Detectors with Prediction-Based Edge Blocking

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Abstract—This paper presents a new phase frequency detector (PFD) to enable fast frequency acquisition in the phase-locked loop (PLL). The three-state PFD is conventionally employed because it is simple and almost immune to the dead-zone problem, but it can miss some rising edges when the edges come during the reset time. Eliminating or reducing the missing edges caused by the reset pulse is essential in achieving fast acquisition. To cope with the missing edge problem, the proposed PFD predicts the reset signal and blocks the corresponding input signal during the reset time. The blocked edge is regenerated after the reset signal is deactivated. Experimental results show that the proposed PFD works correctly for the entire phase difference and achieves 42.1% speed-up in the acquisition time when it is applied to the conventional charge pump PLL implemented in a 0.18μm CMOS technology.

I. INTRODUCTION

The phase-locked loop (PLL) plays the role of generating a clock signal that is usually a multiple of a reference clock and synchronized with the reference clock in phase. The PLL is widely used in many applications such as frequency synthesis, phase modulation, phase/frequency demodulation, and clock data recovery. In most cases, the charge pump PLL (CP-PLL) shown in Fig. 1 is used due to its high frequency range and simple structure [1]-[3]. In the PLL, the phase frequency detector (PFD) compares the rising edges of the reference clock and the voltage-controlled oscillator (VCO) clock, and generates a lead signal when the reference phase is leading or a lag signal when the reference phase is lagging. The phase difference detected in the PFD passes through the loop filter to control the VCO [4][5].

As the phase difference critically affects the overall characteristics of the PLL such as lock-in time and jitter performance, the PFD should be designed to work accurately for any phase difference. However, the PFD suffers from two problems. The first one called the dead-zone problem occurs when the rising edges of the two clocks to be compared are very close. Due to lots of reasons such as circuit mismatch and delay mismatch, the PFD has a difficulty in detecting such a small difference. There have been many PFD structures proposed to cope with this problem. Among them, the three-state PFD shown in Fig. 2 is widely employed because it is simple, easy to implement, and, more importantly, almost immune to the dead-zone problem [6]. Secondly, some of the rising edges can be missed in the detection when the edges are overlapped with the reset signal internally generated in the PFD, which is called the missing edge problem [7][8]. Missing edges induce wrong polarity in the PFD output, leading to incorrect behavior and making the PLL spend more time to acquire phase or frequency. Although the three-state PFD can generate the up (U) and the down (D) signals even if the phase difference is very small, it is not free from the missing edge problem. There have been several research works dealing with the missing edge problem [8]-[10], but most of the previous works require complex circuits or are dedicated to limited cases. As circuit speed increases, the possibility of missing edges increases. Therefore, the missing edge problem becomes a critical factor that determines the acquisition time.

This paper proposes a new PFD to reduce the possibility of missing edges, while maintaining the simple structure provided in the three-state PFD. In order not to lose a rising edge that comes during the reset time, the proposed method predicts the reset signal to delay such a rising edge.

II. MISSING EDGE EFFECTS ON ACQUISITION TIME

In the typical CP-PLL depicted in Fig. 1, the PFD generates the U signal to increase the VCO clock frequency

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when the rising edge of the reference clock comes earlier than that of the VCO clock, and the D signal to decrease the VCO clock frequency when the rising edge of the reference clock comes later than that of the VCO clock. Two conventional three-stage PFD structures are shown in Fig. 2. One is designed using two D flip-flops (D-FFs) and the other is based on the RS latches [6][7]. The two PFDs look different in terms of circuit structure, but they have the same behavior. The PFD makes an either U or D signal when it detects a rising edge of one clock, and maintains the activated signal until the other clock has a rising edge, in other words, it is reset as soon as both U and D signals are activated. Therefore, the width of the generated signal represents the phase difference between the two clock signals. The U and D signals make the charge pump charge upward and discharge downward, respectively.

The PFD should provide the U or the D signal correctly according to the arriving order of the two clock signals, but sometimes it may miss some rising edges. This missing edge problem happens when a rising edge arrives during the reset time, as exemplified in Fig. 3. A rising edge of the VCO clock arrives far earlier than that of the reference clock in the figure, thus the PFD activates the D signal. When a rising edge of the reference clock arrives, the PFD generates a reset pulse to deactivate the D signal. Let us suppose that a new rising edge of the VCO clock arrives during the reset time unfortunately. As the reset pulse overrules the rising edge, the PFD does not detect this rising edge so that it does not activate the D signal that should be generated for the missing edge. In addition, the PFD activates the U signal when an additional rising edge of the reference clock arrives later. Therefore, a missing edge makes the PFD output being reversed in polarity, enlarging the acquisition time of the PLL [8].

Let the reset pulse width and the period of the reference clock are denoted as $T_{\text{reset}}$ and $T_{\text{ref}}$, respectively. The PFD can have wrong polarity if the phase difference is between $2\pi-\Delta$ to $2\pi$, where $\Delta=2\pi\times(T_{\text{reset}} / T_{\text{ref}})$. In the analysis reported in [8], the maximum $\Delta$ is $\pi$, and the maximum reference frequency and VCO clock frequency are limited to $(2\times T_{\text{reset}})$.

To cope with the missing edge problem, several approaches have been developed. The latch-based PFD proposed in [8] generates pulses to replace edges. If a pulse corresponding to the reference clock or the VCO clock is still high when the reset is deactivated, the pulse invokes the U or D signals. Therefore, the circuit is very sensitive on the pulse and the reset pulse and thus it works correctly only when the pulses are controlled properly. There is another PFD that uses two more D-flip flops to check whether or not edges are overlapped with the reset time [9]. If the additional flip-flop detects such a case that an edge is overlapped with the reset signal, it overrides the reset operation to generate output signals of correct polarity. In addition to the two additional flip-flops, it requires pulse generators and more complex flip-flops equipped with two asynchronous inputs of set and clear. Similar to the latch-based PFD, this circuit is also sensitive to the pulse generators and thus it can fail to eliminate the missing edge problem if the pulses are not controlled properly.

**III. THE PROPOSED PFD**

The concept behind the proposed PFD is shown in Fig. 4(a). A switch controlled by the reset signal is connected to each D-FF. The switch is closed when the reset signal is not active and open when the reset signal is activated. The role of the switch is to block the rising edges that may come during the reset time. If the switch is opened, the previous value is maintained by the parasitic capacitor at the D-FF input. Let us assume that a rising edge occurs during the reset time. The rising edge does not appear at the D-FF input, because the switch opened at that time prohibits the edge from propagating to the D-FF input. When the reset time is over, the current value propagates to the FF input, meaning that the switch has an effect of delaying rising edge by the reset time. Therefore, the proposed PFD provides correct polarity even for the edges occurring during the rest time. As the pulse width of the reset signal is very short, we do not need to worry about the charge leakage problem that should be considered in the design of dynamic circuits.
In the implementation, we have to modify the proposed concept because of the delay of generating the reset signal. As the reset signal is generated by passing a rising edge through the D-FF and NAND gate, there is a time difference between the rising edge and the reset signal activation. If a new ringing edge comes during this time difference, it is not possible to block such an edge. Hence, we should open the switch earlier than the reset signal in order to block such a rising edge. For this, we develop a very simple estimation circuit that predicts the reset signal to open the corresponding switch before the reset activation. Suppose that the U signal is high and the D signal is low. In this case, the reset signal is generated only if a rising edge of the VCO clock activates the D signal by passing through the lower D-FF. Therefore when the U signal and the VCO signal are both high, the estimation circuit predicts that the reset signal will be activated soon. This estimation is always correct, and its role is only to generate the reset signal earlier enough to open the corresponding switch. The detailed structure of the proposed PFD is shown in Fig. 4(b).

Compared to the typical three-state PFD, the proposed one requires a few gates and switches additionally, but it is much simpler than the previous PFD proposed for the missing edge problem.

To demonstrate how the proposed PFD works, Fig. 5 shows timing diagrams drawn for two corner cases. The first diagram considers the missing edge case and the other is for the case of small phase difference. In this first diagram, we can see that the edge that rises during the reset time is successfully blocked by the switch and a new edge is regenerated after the reset is deactivated. For the second case, the behavior of the proposed PFD is almost the same as the conventional three-state PFD, as the blocked input signal does not affect the other input signal.

IV. SIMULATION RESULTS

To investigate how the missing edge affects the acquisition time of the CP-PLL, we have performed simulations for various rate of missing edges. For the simulations, the CP-PLL behavior is modeled in C language, including all the components such as the PFD, the Charge Pump and the VCO.

The simulation results are summarized in Fig. 6, where the x axis represents the initial frequency of the VCO and the y axis denotes the average acquisition time to reach the desired frequency of 100MHz. For the sake of easy simulation, the division ratio is set to 1, in other words, the desired frequency is the same as the reference clock frequency. As indicated in Fig. 6, the missing edges rate is a critical factor that determines the acquisition time. In the ideal case that has no missing edges, the acquisition time is much smaller than other cases that have various missing edge rates ranging from 2% to 10%. The more missing edge rate results the longer acquisition time on the average.

Fig. 7(a) shows the frequency characteristics of the proposed PFD, which is obtained by varying the VCO frequency while fixing the reference frequency to 100MHz. When the VCO is slower than the reference, the difference between the accumulated active times of the U and D signals is positive, but it becomes negative when the VCO becomes faster than 100MHz. This is the desired property of the PFD. Fig. 7(b) shows the phase characteristics of the proposed PFD, which is almost linear to the phase difference except the regions close to $2\pi$ or -$2\pi$. Though the difference of U and D signals is not linear but saturated at the region in which the phase difference is large, it keeps the correct polarity. The saturated difference is large enough not to affect the acquisition time, because in such regions the polarity is more important than the magnitude. When the phase difference is small, the magnitude should be linear to the phase difference, as it critically affects jitter performance in the lock-in state. Therefore, the proposed PFD satisfies the desired phase characteristics.
In a 0.18\textmu m technology, we designed two CP-PLLs based on the conventional D-flip flop PFD shown in Fig. 2(a) and the proposed PFD shown in Fig. 4(b) in order to compare their acquisition times. The VCO employed in both implementations oscillates in a range of 1.2GHz to 1.8GHz, and its frequency is controlled by using three capacitors in the coarse tuning step. As the VCO clock is divided by 4 before comparing with the reference clock frequency that is set to 373MHz, the desired output frequency of the VCO is 1.49GHz. Fig. 8 shows the simulation result. During the tracking time in which the VCO tracks the reference clock frequency, the VCO control voltage (Vf) is increasing because the VCO phase is lagging behind the reference clock phase at the beginning. The Vf controls varactors to achieve fine tuning.

When the two frequency values become similar, the Vf converges to a constant value. The proposed PFD takes 28.25\mu s to reach the stabilized Vf, whereas the conventional PFD takes 40.14\mu s because it generates incorrect D signal frequently. The acquisition speed-up achieved by the proposed PFD is as follows.

\[ \text{Speedup} = \frac{T_{\text{old}} - T_{\text{new}}}{T_{\text{new}} \times 100} = \frac{40.14 - 28.25}{28.15} \times 100 = 42.1\% \quad (1) \]

We expect more speedup if the reference clock frequency and the VCO frequency increase, since the possibility of missing edges and thus the possibility of wrong polarity increase in the conventional PFD.

V. CONCLUSIONS

As the missing edge reverses the output polarity of the PFD, it plays a significant role in determining the acquisition time. To achieve fast acquisition by removing the missing edge problem, a new PFD has been presented in this paper. In the proposed PFD, the reset signal is predicted to block the corresponding input signal and the blocked edge is regenerated after the reset signal is deactivated. Experimental results show that the proposed PFD results in 42.1\% speed-up in the acquisition time when applied to the conventional CP-PLL implemented in a 0.18\textmu m CMOS technology. The proposed PFD is simple enough to be implemented with adding a few gates and switches, and more importantly, robust to circuit technology and delay, whereas the previous PFDs presented for the missing edge problem are complex and sensitive to circuit delay, as they are designed based on pulse generators.

REFERENCES