Abstract

In this paper, the effect of power supply noise imbalance on 900MHz differential low noise amplifier (LNA) output is investigated. Chip and package (PKG) power distribution network (PDN) are modeled with lumped components to estimate the power supply noise imbalance. Also an equivalent circuit of differential LNA is modeled to estimate the noise voltage at differential LNA output and verified through measurements. The results of this study reveal that the power supply noise imbalance is mainly caused by impedance resonances of PKG PDN and it directly coupled to the differential LNA output.

Introduction

Not only the basic communication function, but also various kinds of multi-media functions, such as camera, PDA, sensors, video games and so on, are converged into the wireless communication systems to meet the demands of consumers. However, the consumers do not want that the convergences of functions cost extra size; more highly integrated systems are unavoidable. System-in-Package (SiP) and System-on-Chip (SoC) technology can be a solution to realize that highly integrated systems [1]. Through those technologies, more digital circuits to handle the multi-media functions are added on the RF circuits for their basic wireless transceiver function of wireless communication systems.

When the digital circuits are switching, they generate simultaneous switching noise (SSN) on their power distribution network (PDN). Furthermore, it couples to the PDN of RF circuits, which are close to the digital circuits. It degrades the performance of RF circuits. More digital circuits and higher integration with SiP and SoC technologies in the wireless communication systems lead more coupling of SSN on PDN of RF circuits. Accordingly, there are severe performance degradations of the RF circuits.

Among the RF circuits, low noise amplifier (LNA) is one of the essential circuits. It is the first block of the RX front-end. It plays a big role to determine system sensitivity [2]. Also it is very sensitive to noise because it handles very weak RF signals. By this reason, if SSN is coupled on PDN of LNA, it leads not only the severe degradation of the performance of LNA, but also the degradation of system sensitivity. To reduce the noise sensitive characteristic of LNA, differential structure has been widely used. Previous reported studies of the effect of noise on differential LNA focus on the common-mode noise rejection characteristic of differential structure [3] or the on-chip substrate noise [4]. This paper investigates that if the power supply noise on PDN of differential LNA for 900MHz application, which is coupled from SSN on package (PKG) PDN of digital circuits, is not common-mode noise at each half-circuit of differential LNA, how much noise is coupled out to differential output of LNA. For the investigation, PDN of chip and PKG are modeled with lumped components to estimate the power supply noise at each half circuit of differential LNA. Also an equivalent circuit of LNA is modeled to estimate the noise voltage at differential LNA output and verified through measurements.

Power Supply Noise Imbalance on Differential LNA

It can be assumed that there is a differential LNA, which is composed of two symmetric single-input/output half-circuits. Each half-circuit has its own power/ground (P/G) nodes and they are tied by on-chip PDN.

If the on-chip PDN is ideal, tied P/G nodes of half-circuits by on-chip PND are exactly same nodes. As shown in fig. 1 (a), power supply noise on on-chip PDN of differential LNA, which is from SSN on PDN of digital circuits, is same at P/G nodes of each half-circuit. Therefore, the common-mode power supply noise is easily rejected at the differential output of LNA.

But in real world, every metal line of on-chip PDN has R, C parasitics. Furthermore, the LNA usually has large PDN because of large inductors on chip, P/G nodes of each half-circuit cannot be the same nodes. There will be difference between amounts of power supply noise on each P/G nodes. Accordingly, the supply noise is coupled out to the differential output of LNA as shown in fig. 1 (b). In this paper, this noise imbalance at P/G nodes of each half-circuit of differential LNA is defined as power supply noise imbalance.

Fig. 1 (a) Power supply noise on ideal on-chip PDN of differential LNA (b) power supply noise on real on-chip PDN of differential LNA: Power supply noise imbalance

Models to Investigate the Effect of Power Supply Noise Imbalance on 900MHz Differential LNA

To investigate the effect of power supply noise imbalance on 900MHz differential LNA, on-chip/PKG PDN and an equivalent circuit of differential LNA are modeled with lumped components. Through the models, power supply noise imbalance...
imbalance at each half-circuit of differential LNA and the noise voltage at differential LNA output are estimated.

Fig. 2 Test vehicle (a) Schematic and die-photo of 900MHz differential LNA (b) PKG for differential LNA

Fig. 2 shows test vehicle. The differential LNA is common-source amplifier with source degeneration. It has ring type on-chip PDN of $1.2 \times 1.1\text{mm}$ and perfectly balanced layout except single bias line. As shown in fig. 2 (a), the LNA is composed of two symmetrical half-circuits. Each half-circuit has its own P/G nodes and P/G bond-wire pads. They do not connect each other at schematic level. But they are tied by on-chip PDN of the LNA. The PKG for the LNA has size of $66\text{mm} \times 26\text{mm}$ as shown in fig. 2 (b). PKG PDN is composed of power/ground plane with same size of PKG, which are placed at 2nd, 3rd floor of PKG. The LNA is placed at the center of top level of the PKG. 2 pairs of P/G bond-wire, which connect PKG PDN and on-chip PDN, are placed at side of both half-circuits of LNA. DC power to operate LNA and P/G noise, which is assumed as power supply noise on PKG PDN coupled from SSN of digital circuits, are excited at P/G noise input port on right side of PKG.

**A. PKG PDN Model**

The PKG PDN is modeled with balanced transmission line matrix (TLM) method as shown in fig. 3. TLM is a method which models planes in several unit cells [5]. Each cell is considered as a piece of transmission line and modeled with R, L, C, G lumped elements. The size of unit cell should be kept under $\lambda/20$ of maximum target frequency of modeling, since the modeling with lumped elements is only effective when there is no voltage variation at inside of unit cell. In this paper, all models are modeled from 100MHz to 2GHz. Hence, the size of unit cell of PKG PDN is determined as 2mm which covers the maximum target frequency of modeling.

**B. On-chip PDN Model**

On-chip PDN of the differential LNA is modeled with R, C components as shown in fig. 4. As similar as TLM method, each ring of on-chip PDN is divided with 30um square unit cell. The unit cell contains conductor loss of on-chip metal and coupling capacitance between power and ground cell. The area and fringing capacitance between power/ground cell and silicon substrate are ignored. Because the distance and coupling capacitance between power/ground cell and silicon substrate are 4 times smaller than those between power and ground cell. Also the inductance of the unit cell is ignored because the effects of inductance are not significant under the maximum target frequency of modeling: 2GHz. 48pF decoupling capacitor is distributed around the on-chip PDN and added on the on-chip PDN model.

**C. Equivalent Circuit Model of Differential LNA**

Equivalent circuit of differential LNA is modeled by replacing 4 NMOSs in the schematic of the LNA with equivalent MOS model for high frequency as shown in fig.6. Equivalent MOS model includes gate-drains, gate-source and drain-source capacitance to cover the characteristics of MOS in high frequency region [6].

**Analysis of the Effect of Power Supply Noise Imbalance**

When a noise voltage is excited at P/G noise input port on PKG, at first, it propagates through PKG PDN. Then the P/G
bond-wire pairs, which are placed side by side of both half-circuits of the differential LNA, pick up the noise at their position on PKG PDN. The coupling paths from P/G noise input port to P/G bond-wire pairs through PKG PDN have 2mm length difference as shown in fig. 2 (b). P/G noise picked up by + P/G bond-wire pair propagates one more unit cell of PKG PDN model than P/G noise picked up by − P/G bond-wire pair. This difference causes different amount of noise voltages at each P/G bond-wire pair. Although the P/G bond-wire pairs are tied together by on-chip PDN of LNA, there are many cells of on-chip PDN model between +− P/G bond-wire pads of on-chip PDN: those P/G bond-wire pads are directly connected to P/G nodes of +− half-circuits. This is the main reason of power supply noise imbalance.

The power supply noise imbalance between half-circuits of differential LNA is estimated through the models. First, it is assumed that there is $V_{P/G\_noise}$ at the P/G noise input port on PKG. Next, $V_{P+}$, $V_{P−}$, $V_{G+}$ and $V_{G−}$ which are the noise voltages at P/G nodes of +− half-circuits on on-chip PDN of LNA, are obtained through Spice simulations with the models. $V_{P+}$ represents power node of +half-circuit and G- of $V_{G−}$ represents ground node of − half-circuit. The transfer functions between P/G noise input port on PKG and the P/G nodes are defined as equation (1). Then, transfer function of power supply noise imbalance is expressed as equation (2) and plotted at fig. 6.

$$T_{P+} = \frac{V_{P+}}{V_{P/G\_noise}}, \quad T_{P−} = \frac{V_{P−}}{V_{P/G\_noise}}$$

$$T_{G+} = \frac{V_{G+}}{V_{P/G\_noise}}, \quad T_{G−} = \frac{V_{G−}}{V_{P/G\_noise}}$$

(1)

$$T_{PSNI\_Pwr} = \frac{V_{P+}−V_{P−}}{V_{P/G\_noise}}, \quad T_{PSNI\_Gnd} = \frac{V_{G+}−V_{G−}}{V_{P/G\_noise}}$$

(2)

Fig. 6 shows that if there is 1V of 1.5GHz single-tone noise at P/G noise input port on PKG, 0.28V of noise voltage difference will be at between power nodes of +− half-circuits, and 0.32V of noise voltage difference will be at between ground nodes of +− half-circuits. The power supply noise imbalance varies with frequency of P/G noise at input port on PKG. Fig. 6 (a) and (b) shows that the power supply noise imbalance increases around 200MHz, 500MHz, 1GHz and 1.5GHz. This is because of the impedance resonances of PKG PDN. The first peak around 200MHz is from series resonance between L of power supply and C of bias tee which is used to excite DC and P/G noise at P/G noise input port on PKG. The second one is from series resonance between inductance and capacitance of PKG PDN. The third and forth ones are from cavity resonance of PKG PDN.

Estimation and Experimental Verification of the Noise Voltage at Differential Output of LNA caused by the Power Supply Noise Imbalance

Due to the power supply noise imbalance, phase and magnitude of noise voltage differs from a noise supplied to +half-circuits of differential LNA to a noise supplied to − half-circuits. These noises are not common-mode noise anymore. Therefore, the P/G noises are coupled to differential output of LNA. Solid line of fig.8 is the simulated result of a noise voltage at differential output of LNA with models when there is 50mV AC noise at P/G noise input port on PKG. From the simulation result, we can verify that power supply noise imbalance directly causes the peaks around 200MHz, 500MHz, 1GHz and 1.5GHz which are in the light-gray boxes. The other peaks around 1.1GHz and over 1.6GHz, which are in the dark-gray boxes, are from a gain error of output balun. Because the output balun is for 900MHz applications, it has a gain error at the other frequencies. The latter peaks are out of our interests.
The simulation result is verified with measurement. Fig. 7 shows the measurement setup. DC power and single-tone P/G noise are excited at P/G noise input port on PKG through a bias tee. The frequency of P/G noise sweeps from 100MHz to 2GHz. The output power of signal generator, which is the source of P/G noise, is controlled to always fix the magnitude of P/G noise voltage into input port of PKG as 50mV at every frequency point. Input port of LNA is 50ohm terminated. Then, a real-time spectrum analyzer measures the noise at differential output of LNA. The measurement result is shown at dashed-stems with circle points at fig. 8. From the comparison between the simulation and measurement result, it is shown that the frequency point and magnitude of peaks of them show same tendency. Consequently, we can conclude that the simulation of noise voltage at differential output of LNA caused by the power supply noise imbalance through the models is verified with measurement.

![Fig. 7 Measurement setup](image)

![Fig. 8 Noise voltage at differential output of LNA](image)

**Conclusions**

This paper has investigated the effect of power supply noise imbalance on differential circuit, in particular the differential LNA for 900MHz application. First, the effects of power supply noise imbalance are proposed. Next, on-chip/PKG PDN and equivalent circuit of LNA are modeled with lumped components. The analysis of the power supply noise imbalance through the models indicates that the power supply noise imbalance is caused by as following reasons: 1) the length difference of coupling paths between P/G noise input port on PKG and P/G bond-wires of half-circuits of the LNA through PKG PDN and 2) R, C parastics between +/- P/G bond-wire pads of on-chip PDN. The simulations through the models indicate that the power supply noise imbalance is mainly affected by impedance resonance of PKG PDN. Finally, simulation and measurement result of the noise voltage at differential LNA output show that the power supply noise imbalance is directly coupled out to the differential output of LNA and affected by the impedance resonance of PKG PDN.

The investigation of the effect of power supply noise imbalance on differential LNA in this paper indicates that, depends on the design of PKG PDN and the size of on-chip PDN, the differential structure is not always safe at the aspect of power supply noise rejection.

**References**


