A 12-bit Segmented DAC with a Serial Voltage Adder for AMLCD Column Drivers

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ABSTRACT

In this paper, a 12-bit linear segmented type digital-to-analog converter (DAC) for application to AMLCD column drivers is presented. The proposed DAC includes a global resistor string, six 2-bit sub-DACs, and a serial voltage adder. The serial voltage adder can generate final voltage in only three cycles through use of the charge subtraction concept. Simulation results based on 0.35um high voltage CMOS technology show an INL of less than 0.7LSB and a DNL of less than 0.3LSB.

1. INTRODUCTION

The cathode ray tube (CRT) has nearly disappeared due to its huge size and large power consumption and the use of flat panel displays (FPDs) is accordingly expected to rapidly increase. In the FPD market, active matrix organic light emitting diodes (AMOLEDs) have recently garnered much attention. Nevertheless, active matrix liquid crystal displays (AMLCDs) are still thriving commercially, especially in large size panel applications. A larger screen, higher resolution, and higher color depth are required to stay in step with the current trend of LCD panels. A LCD driver IC is also required to provide the aforementioned high performances.

Owing to increased resolution, 1-horizontal (H) time is getting shorter. For example, the 1-H time of a 60Hz full high-definition (HD) resolution (1920 1080) panel is around 15us. The 1-H time will be reduced by half or by a factor of four in a 120Hz or 240Hz frame rate panel, respectively, which means the column driver IC settling time must be accordingly decreased. Furthermore, this problem is exacerbated with increasing panel size. In terms of high quality color, 10bit color depth and RGB independent gamma correction are required to produce natural and rich colors. Due to these mentioned reasons, it is essential to increase the resolution of the DAC.

A conventional resistor string DAC (R-DAC) has been successfully used as 6 or 8 bit driver ICs. However, the occupied area exceeds more than 60% of the overall driver IC due to the large size decoder and corresponding reference voltage routing lines [1]. Under these circumstances, it is difficult to apply a R-DAC with more than 10bit resolution, because the DAC size increases roughly twofold as the resolution increases by 1bit. Therefore, reducing the area of the DAC is the main design issue in driver ICs.

In efforts to resolve the DAC size problem, various interpolation methods have been introduced, wherein most significant bit (MSB) is performed in the resistor string and the remaining least significant bit (LSB) in the interpolation part [1]-[6]. The interpolation is performed by binary weighted capacitors [2], a current DAC [1], [3] or an interpolation amplifier consisting of multiple input transistors [4], [5]. Nevertheless, the size of the decoder and the routing lines remains large, because the decoder should deal with many bits. Another approach was presented in [6] named cyclic DAC (C-DAC) which is much more area efficient due to the use of only two identical capacitors and several switches. However, the conversion time is quite long, especially in high resolution, because digital to analog conversion is performed at 1bit/cycle. A segmented DAC that uses several small decoders instead of one large decoder to reduce the area occupied by the decoders was also recently proposed [7], [8].

In this paper, six 2-bit decoders are used to further reduce the area of a previously reported segmented DAC. In addition, a serial voltage adder is adopted to reduce the number of capacitors. By using the charge subtraction concept, the conversion time is reduced by half.
2. CONCEPT OF SEGMENTED DAC ARCHITECTURE

A conceptual diagram of segmented DAC architecture is presented in Figure 1. The proposed DAC consists of a global resistor string, six 2-bit decoders, a voltage adder, and a unity gain output buffer. Previous works applied two 6-bit decoders or three 4-bit decoders whereas the proposed DAC applies six 2-bit decoders and its size is thereby reduced by half.

The global resistor string generates a total 24 reference voltages. 12 bit digital input code is divided into six 2-bit codes and each of the 2-bit codes is used to select the corresponding reference voltage from the global resistor string. The output voltages of the six 2-bit decoders are:

\[ V_6 = \frac{V_{\text{gamma}}}{2} D_{1,10} \]  
\[ V_5 = \frac{V_{\text{gamma}}}{2^2} D_{6,8} \]  
\[ V_4 = \frac{V_{\text{gamma}}}{2^2 \cdot 2^2} D_{7,6} \]  
\[ V_3 = \frac{V_{\text{gamma}}}{2^3 \cdot 2^2} D_{8,4} \]  
\[ V_2 = \frac{V_{\text{gamma}}}{2^3 \cdot 2^2 \cdot 2} D_{9,2} \]  
\[ V_1 = \frac{V_{\text{gamma}}}{2^4 \cdot 2^2 \cdot 2^2} D_{10,0} \]  

where \( D_{1,k} = 2^k D_k \). The final output voltage is obtained by adding the six voltages selected by the 2-bit decoders. The final output voltage is:

\[ V_{\text{out}} = \frac{V_{\text{gamma}}}{2^{12}} (2^{10} D_{1,10} + 2^9 D_{6,8} + 2^8 D_{7,6} + 2^7 D_{8,4} + 2^6 D_{9,2} + 2^5 D_{10,0}) \]  

At least six capacitors are required when six voltages are summed by the conventional switched capacitor (SC) type adder. A DAC that uses capacitors is influenced by capacitor mismatch. To reduce the effect of capacitor mismatch, the capacitor size should be enlarged. However, this places a burden on DAC size. A new approach focused on reducing the number of capacitors is thus needed.

3. CIRCUIT DESIGN OF THE PROPOSED DAC WITH A SERIAL VOLTAGE ADDER

The proposed segmented DAC with a serial voltage adder (SVA) is shown in Figure 2. It consists of a global resistor string, six 2-bit decoders, and a SVA for summation of decoder output voltages.

Due to the serial adding function, the SVA basically needs two capacitors: a sampling capacitor, \( C_S \) which samples the decoder output voltage and holding capacitor, \( C_H \) which stores charge transferred from \( C_S \). Additional capacitor \( C_{\text{off}} \) is used for op-amp offset cancellation. If the SVA performs adding via the conventional approach, 6 cycles are needed to add the voltages of six decoders. Even though the conversion time is half that compared with a C-DAC, it is still insufficient to drive in 1-H time. The SVA in the proposed...
architecture can complete the serial summation in only 3 cycles by adopting the charge subtraction concept [9]. In the conventional approach, for example, all charge sampled by \( C_s \), thus corresponding to \( V_X \), is delivered to \( C_{an} \). On the other hand, with application of the charge subtraction concept, only the amount of certain charge sampled by \( C_s \) is delivered to \( C_{an} \) which will be \( V_{X}-V_{Y} \).

The proposed DAC operates in 2 steps: a conversion step and a driving step. The conversion step can be divided into 3 cycles. In the first phase of the first cycle, \( P1 \) switch is turned on and \( C_{off} \) is initialized. \( C_{off} \) is connected to both side inputs of the op-amp and then samples the offset voltage of the op-amp. At the same time, \( P2 \) and \( P3 \) switches are turned on and the \( V_{H2}-V_{GM} \) voltage is sampled in \( C_s \). In the second phase of the first cycle, \( P1 \) switch is turned off and \( C_{off} \) is connected between the positive input of the op-amp and the \( V_{GM} \) node to cancel the offset of the op-amp, and thus voltage of node \( X \) shown in Figure 2 will be \( V_{GM} \). After that, \( P2 \) and \( P3 \) switches are turned off and some portion of the charge sampled by \( C_s \) is delivered to \( C_{an} \) which will be \( V_{X}-V_{H1} \) by turning on \( P3-1 \) switch. In the second cycle, \( C_{off} \) is still connected between the positive input of the op-amp and the \( V_{GM} \) node, and thus voltage of node \( X \) is maintained as \( V_{GM} \). \( P4 \) switch is turned on in the first phase of the second cycle, and in the next phase \( P4 \) is turned off and \( P4-1 \) is turned on so that some portion of the charge sampled by \( C_s \) is delivered to \( C_{an} \) which will be additionally charged as much as \( V_{M2}-V_{M1} \). In the third cycle, a similar procedure is performed and \( C_{an} \) will be additionally charged as much as \( V_{H2}-V_{H1} \). After finishing 3 cycles, finally, \( V_{H2}-V_{H1}+V_{M2}-V_{M1}+V_{X}-V_{H1} \) voltage is charged in \( C_{an} \). In the driving step, \( P0 \) switch is turned on and the panel load is driven by the unity gain buffer amplifier in the SVA. Finally, the voltage of the panel load will be the sum of the voltage charged in \( C_{an} \) and \( V_{GM} \).

In the first cycle, the settling time is longer than that in the second cycle or third cycle due to the sampling and holding action of higher voltage. To use the buffer amplifier as an op-amp in the SVA without any performance enhancement consuming more current, the period of the first cycle is designed to be two times longer than that of the second or third cycle. The period of the first cycle and second cycle is 2us and 1us, respectively. The period of the third cycle is the same as for the second cycle. Therefore, the total conversion time of the proposed DAC is 4us.

Reference voltages selected by the decoder differ slightly from that given in section 2 due to use of the charge subtraction concept. The output voltages of the six 2bit decoders and the final output voltage of the proposed DAC are obtained as follows:

\[
V_{H1} = \frac{V_{REF}}{2^2}(D_{11,0} + 1) + V_{GM} \tag{8}
\]

\[
V_{H2} = \frac{V_{REF}}{2^2}(D_{11,1} + 1) + V_{GM} \tag{9}
\]

\[
V_{M1} = \frac{V_{REF}}{2^2}(D_{11,0} + 1) + V_{GM} \tag{10}
\]

\[
V_{M2} = \frac{V_{REF}}{2^2}(D_{11,1} + 1) + V_{GM} \tag{11}
\]

\[
V_{L1} = \frac{V_{REF}}{2^2}(D_{11,0} + 1) + V_{GM} \tag{12}
\]

\[
V_{L2} = \frac{V_{REF}}{2^2}(D_{11,1} + 1) + V_{GM} \tag{13}
\]

\[
V_{M32} = V_{H1} + V_{M2} - V_{M1} + V_{L2} - V_{L1} + V_{GM}
\]

\[
= \frac{V_{REF}}{2^2} \left( 2^{10}D_{11,0} + 2^4D_{11,1} + 2^8D_{11,6} \right) + V_{GM} \tag{14}
\]

Finally, owing to application of the charge subtraction concept in the SVA, the proposed DAC successfully converts digital input data to corresponding analog voltage by adding six voltages of decoders in only 3 cycles.

4. SIMULATION RESULTS

The proposed linear 12bit segmented DAC with a serial voltage adder was designed in 0.35um high voltage CMOS technology. Cadence SPECTRE™ is used as the simulation tool. A 3.3V supply is applied in the logic part and a 12V supply is applied in the analog part. The positive gamma range is from 6.2V to 11.8V and the negative gamma range is from 0.2V to 5.8V. Accordingly, 1 LSB magnitude is 1.367mV.

A rail to rail input and class AB output amplifier topology [3] is modified for the op-amp, which is also used for the output buffer in the SVA. A NMOS input op-amp for the positive gamma range, and a PMOS input op-amp for the negative gamma range, are respectively designed. The op-amp for positive gamma consumes quiescent current of 6.5uA, and the op-amp for negative polarity consumes 6uA.

To demonstrate the performance of the proposed DAC, the digital ramp signal from 000000000000 to 111111111111 is applied with an equivalent panel load, which consists of 6K\( \Omega \) and 300pF, as shown in Figure 2. At the input node of the panel load, the maximum time for the output to settle in 1LSB of the final output voltage was 10us including 4us conversion time. Figures 3 and 4 shows simulation results of INL and DNL for a positive gamma range and negative gamma range, respectively. The maximum INL and DNL for the positive gamma range are obtained as follows:

\[
V_{H1} = \frac{V_{REF}}{2^2}(D_{11,0} + 1) + V_{GM} \tag{9}
\]

\[
V_{H2} = \frac{V_{REF}}{2^2}(D_{11,1} + 1) + V_{GM} \tag{10}
\]

\[
V_{M1} = \frac{V_{REF}}{2^2}(D_{11,0} + 1) + V_{GM} \tag{11}
\]

\[
V_{M2} = \frac{V_{REF}}{2^2}(D_{11,1} + 1) + V_{GM} \tag{12}
\]

\[
V_{L1} = \frac{V_{REF}}{2^2}(D_{11,0} + 1) + V_{GM} \tag{13}
\]

\[
V_{M32} = V_{H1} + V_{M2} - V_{M1} + V_{L2} - V_{L1} + V_{GM}
\]

\[
= \frac{V_{REF}}{2^2} \left( 2^{10}D_{11,0} + 2^4D_{11,1} + 2^8D_{11,6} \right) + V_{GM} \tag{14}
\]
range are 0.3LSB and 0.3LSB, respectively, and the maximum INL and DNL for the negative gamma range are 0.7LSB and 0.2LSB, respectively. The difference between positive polarity and negative polarity may be due to the difference in the op-amp performances. Table 1 presents a performance summary.

5. CONCLUSION
An area efficient linear 12bit segmented DAC with a serial voltage adder scheme has been proposed for application to AMLCD column drivers. Instead of using one large decoder, the proposed DAC uses six small 2-bit decoders to reduce the area occupied by the decoders. In addition, the charge subtraction concept is applied to the serial voltage adder in order to reduce the number of capacitors and the conversion time.

Table 1 Performance summary

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Performance (simulation)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gray level</td>
<td>12-bit linear</td>
</tr>
<tr>
<td>Voltage supply</td>
<td>3.3V (logic), 12 V (Analog)</td>
</tr>
<tr>
<td>Settling time</td>
<td>10 us (include 4us conversion time)</td>
</tr>
<tr>
<td>Panel load</td>
<td>6KΩ + 300pF</td>
</tr>
<tr>
<td>INL/DNL</td>
<td>0.7/0.3 LSB</td>
</tr>
<tr>
<td>Power consumption</td>
<td>6.5 uA/channel</td>
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<tr>
<td>Display application</td>
<td>Large size 60Hz full-HD resolution</td>
</tr>
<tr>
<td>Technology</td>
<td>0.35um CMOS</td>
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</tbody>
</table>

As a result, the proposed linear 12-bit DAC has reduced overall area compared to the conventional 8-bit R-DAC and completes the conversion in only 3 cycles. Simulated INL and DNL values are less than 0.7LSB and 0.3LSB, respectively. The proposed DAC is applicable to a 60Hz large size full-HDTV panel having a 1-H time of around 15us.

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REFERENCES