4.5 A Fully Integrated Dual-Mode CMOS Power Amplifier for WCDMA Applications

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Integrating a CMOS RF power amplifier (PA) into a single-chip transceiver is one of the most challenging works in implementing radio front-ends, which presents many advantages in handheld applications [1,2]. Especially, low-power efficiency enhancement (LPEE) techniques, considering the probability distribution function of the practical wireless communication environments, extend the battery lifetime in handheld devices [1-3]. Therefore, there are many studies for the LPEE in handheld CMOS PAs [1,2] using transmission-line transformers (TLTs) with parallel amplifiers. Designing a series/parallel-combining transformer (SCT/PCT) is one of the key factors in the implementation of a dual-mode CMOS PA. However, the dual-mode performances of the PA must be optimized by using one output TLT structure. It is expected that there are difficulties in designing a highly efficient dual-mode PA. Therefore, this paper introduces a fully integrated dual-mode CMOS PA with a proposed output TLT with 2 control switches, which allows an LPEE with a back-off region of 10dB or more with a very low quiescent current.

Figure 4.5.1 shows a simple schematic of the dual-mode TLT. The output power from a differential amplifier is combined to the RF output by the magnetically coupled TLT in the high-power mode (HPM). The secondary line of the TLT is directly connected to a single-ended amplifier for LPM operation. It is different from the previous SCT/PCT designs of dual-mode CMOS PAs [1,2]. The proposed TLT has advantages in efficiency and implementation area with which a 1/10 sized low-power transistor is used for the LPEE with a back-off region of 10dB or more. For an LPM amplifier, we use a single-ended amplifier instead of a differential one. Because the real part of the optimum impedance for the HPM differential amplifier is 18Ω (9Ω at each drain), that for the LPM differential amplifier becomes 180Ω (18×10). However, the single-ended LPM amplifier requires 45Ω (9×5) at the drain. In terms of designing an output matching network from the RF output (50Ω) to the optimum impedance at the drain of the LPM amplifier, the single-ended amplifier is better than a differential one.

The mode change in the output matching network is realized by 2 shunt switches, SW_1 and SW_2 . If we use series switches for dual-mode operation, the insertion loss, reliability and isolation of the CMOS switch will be problematic. Therefore, 2 shunt switches, realized with two 4mm stacked transistors with a large resistor of $16k\Omega$ at the gate and body terminals [4], are used. These shunt switches also help complete the output matching network. Without SW_1 , the impedance moves to a low impedance Z_1 for the HPM due to the use of C_2 instead of the high impedance, as shown in Fig. 4.5.1. This complicates the LPM output matching. Thus, the SW_1 creates a high impedance at the drain of a small LPM amplifier to enhance the performances in the large back-off region.

Figure 4.5.2 shows that the integrated bias circuits for CS and CG amplifiers in the cascode structure help enhance the linearity and efficiency of the CMOS PA in [5]. The reshaped envelope signal injection to the gate of the CS restores the distortion of the PA output at the peak of the envelope signal. This reduces the spectrum regrowth, IMD or ACLR, and enhances the efficiency at low powers as well as at maximum linear power. Additionally, the bias circuit at the CG amplifier, a proper R-C-L network, controls the impedance for the 2nd-order nonlinear components (Δf and $2f_0$) to reduce the sideband asymmetry and its magnitude in the PA.

Figure 4.5.3 shows a schematic of the dual-mode amplifier. All matching networks and linearization bias circuits are integrated on a chip. To moderate the voltage stress in each low-breakdown-voltage transistor and reduce the effects of bonding wires at the source of the amplifier, a differential cascode structure is widely used in the design of a CMOS PA [1,2]. In contrast to an HPM amplifier, the effect of the package parasitic is not a major problem in a single-ended LPM amplifier. The feedback networks, R_{F1} , R_{F2} , C_{F1} and C_{F2} , are used to improve the stability and the linearity of the PA. The gate lengths of MD_1/MP_1 and MD_2/MP_2

are both $0.18\mu m$ and that of the thick oxide device is $0.4\mu m$. The total gate widths of MD_1 , MD_2 , MP_1 and MP_2 are 768, 1024, 4096 and $5120\mu m$, respectively.

An inter-stage BALUN completes the matching and feeds the drain bias with an AC virtual ground in the primary line for fundamental frequency (f_0) and odd-order harmonics. An AC virtual ground node of the secondary line is also used for biasing, to transmit the reshaped envelope signal to the gate of the power stage. The input BALUN completes the input matching and feeds the driver stage gate bias from the output of the linearization CS bias circuit. The on-chip TLT is implemented using stacked-metals, copper and aluminum, connected through whole copper via traces. Both lines of the output TLT are separated into two parts to reduce the insertion loss by increasing the coupling factor. The insertion loss of the output matching network including the 2 switches, which have a loss of 0.23dB due to the on-resistance, in LPM/HPM is simulated to be 1.52/1.3 dB at 1.95GHz.

Because the single-ended LPM path shares the path of the differential CS amplifier in the HPM driver stage, the input BALUN and the linearization CS bias circuit for the HPM can be commonly used in the LPM amplifier. Therefore, the additional single-ended parallel amplifier for LPM does not increase the implementation size and complexity. For the mode change, control of the gate bias of the CG amplifiers and 2 switches are needed as shown in Fig. 4.5.3. Turning off the CG amplifier saves the quiescent current and helps improve the stability and isolation due to removal of the feedback path. As the watt-level output power in the HPM is degraded by leakage in the additional LPM path through the body of the LPM CG amplifier, a large resistor ($16k\Omega$) at the body terminal in the LPM CG amplifier is used to improve the isolation when V_{CG3} is off [4]. Contrary to the two-stage HPM amplifier, the one-stage LPM amplifier has a smaller gain. However, if the decrease in gain is less than that of the output power between the two different modes, there is no additional burden in the transmitter when driving the LPM amplifier.

A fully integrated dual-mode RF PA was fabricated in $0.18\mu m$ CMOS technology (Fig. 4.5.7). The quiescent current of the PA for each mode is 57mA (HPM) and only 20mA (LPM) with a supply voltage of 3.4V. Figure 4.5.4 shows the simulated and measured dual-mode S-parameters versus frequency. The power gain is 23.7dB in the HPM, and 12.6dB in the LPM at 1.95GHz. As mentioned before, because the mode change components remove the feedback paths, which are oscillation sources in each mode, the dual-mode linear PA secures the stability. Figure 4.5.5 shows the measured gain and PAE versus the output power with a CW test, the measured ACLR at a 5MHz offset versus the average output power using a 3GPP WCDMA signal, and its spectrum at 1.95GHz. In the CW test, the peak power is 20.2/30.5dBm with a PAE of 33.9/42.1% in the LPM/HPM. The maximum output power satisfying the WCDMA linearity specification with 2dB margins, -35dBc, is 16.4/28.0dBm with a PAE of 27.4/36.4% in the LPM/HPM. Figure 4.5.6 shows the comparison table with published state-of-the-art dual-mode PAs.

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Figure 4.5.1: Simplified schematic of the dual-mode output matching network and impedance traces with/without SW₁ during LPM operation.

Figure 4.5.2: Integrated CS and CG bias circuits for linearization in the cascode PA.

Figure 4.5.3: Schematic of the fully integrated dual-mode CMOS PA.

Figure 4.5.4: Simulated and measured S-parameters for the dual-mode operation when the P_{IN} is -20dBm.

Figure 4.5.5: Measured power gain and PAE for the CW signal, ACLRs and currents for a WCDMA signal with respect to average P_{OUT} at 1.95GHz, and its output spectrum when the average P_{OUT} is 28 dBm.

	Ref. [3]	Ref. [1]	This Work
Technology	InGaP/GaAs HBT	0.18μm CMOS	0.18μm CMOS
Frequency	1.95GHz	2.5GHz	1.95GHz
Application	WCDMA	WLAN/WiMAX	WCDMA
V _{DD}	-	3.3V	3.4V
Quiescent current	-	LPM : 105mA HPM : 590mA	LPM : 20mA HPM : 57mA
CW test	P _{SAT}	LPM* : 22.0dBm HPM : 31.0dBm	LPM : 20.2dBm HPM : 30.5dBm
		LPM* : 15.2% HPM : 34.8%	LPM : 33.9% HPM : 42.1%
WCDMA test	P _{in}	LPM : 16dBm HPM : 28dBm	LPM : 16.4dBm HPM : 28.0dBm
	PAE @ P _{in}	LPM : 21.0% HPM : 44.5%	LPM : 27.4% HPM : 36.4%
	ACLR @ P _{in}	-38dBc (5MHz offset)	-35dBc (5MHz offset)
Output Matching	Off-chip Components	On-chip TLT (PCT)	On-chip TLT (Proposed)
Etc.	Balanced PA	MPM* is existed (26.7dBm with 23%)	Integrated bias ckts for linearization

*Values taken from Fig. 14 of [1]

Figure 4.5.6: Comparison table with published state-of-the-art dual-mode PAs for LPEE.

Figure 4.5.7: Die photo of the PA in 0.18μm CMOS (1334×2044μm²).