LLC Series Resonant Converter with Auxiliary Hold-Up Time Compensation Circuit

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***Abstract*-- LLC series resonant converter is the most attractive topology for medium power application due to its high efficiency and wide input range. Despite these advantages, it is difficult to optimally design to satisfy hold-up time requirement, and it reduces efficiency of the converter and power density is degraded because of bulky magnetizing components. To solve these drawbacks, LLC series resonant converter with auxiliary hold-up time compensation circuit is proposed. By using auxiliary hold-up time compensation circuit, the LLC converter gets higher gain when hold-up of output voltage is required, and the efficiency of the converter can be improved by the optimal design in normal operation mode. In this paper, operational principle of the proposed circuit is presented and experimental results with prototype are given to confirm the validity of the proposed circuit.**

***Index Terms*—LLC resonant converter, hold-up time**

I. INTRODUCTION

With the development of power conversion technology, power density and efficiency of converter has become the major challenge [1],[2]. In AC/DC adapter application, as customers need the compact adapter, higher power density and efficiency is required to meet customers' needs. Fig. 1 shows the structure of AC/DC adapter, and it consists of AC/DC converter and DC/DC converter [3]. The first AC/DC stage provides dc link voltage with power factor correction (PFC) and the DC/DC converter stage tightly regulates an isolated output voltage. Besides high power density and efficiency, the AD/DC adapter also requires a hold-up time specification [4]-[7]. The adapter should provide output voltage for dozens of milliseconds after loss of AC input under full load condition. To satisfy hold-up time requirements, the link capacitor size, which is placed between PFC and DC/DC converter, becomes larger, but it is a retrogressive approach from the viewpoint of high power density. Therefore, the DC/DC converter needs to be designed with a wide input range for high power density [9]-[13].

Among many DC/DC converter topologies, LLC series resonant converter is the most attractive topology due to its high efficiency and wide input range [4]-[13]. Fig. 2 shows the circuit diagram of conventional LLC series resonant converter. Generally, LLC resonant converter operates optimally with high efficiency when the switching frequency and the resonant frequency of L_R ,C_R are equal [6]. At this point, because the impedance of a resonant tank becomes zero, the input and output voltages are virtually connected and its AC voltage gain is unity [6]. In normal operation conditions, the input voltage of the converter is regulated to 400V by PFC stage. With the regulated input voltage and unity gain at resonant frequency, the transformer turns ratio can be chosen and the magnetizing inductance of transformer also can be designed to guarantee the zero voltage switching for primary switches [4]-[13]. However, it is difficult to optimally design the resonant tank of L_R and C_R to satisfy hold-up time requirements. To obtain high voltage gain for hold-up time, the operating frequency moves downward far from the resonant frequency [9]-[11]. This results in bulky magnetizing components and low efficiency by large circulating current. To adjust more gain with small switching frequency variation, large L_R or small L_m can be designed but it lowers power density and efficiency of the converter [9]-[11]. In other words, performance of the converter will be degraded to meet hold-up time requirements.

To solve these problems, several methods have been studied [1]-[8]. For example, a baby boost converter is inserted in conventional PFC converter to extend the hold-up time [2]. In case the AC line lost, the baby boost converter increases the link voltage [2]. However, additional power diode in main current path decreases the converter efficiency. Moreover, the power density is also decreased by an additional inductor. In reference [7], integrated inductor approach is used for high power density, but power semiconductor devices with high voltage rating and additional bulky capacitor are still required. Several hold-up time compensation methods on

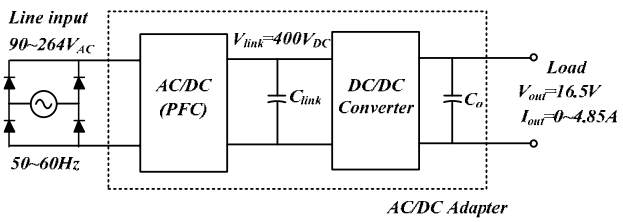

Fig 1: Structure of AC/DC Adapter

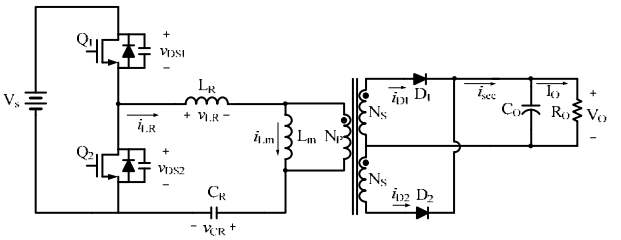

Fig 2: Circuit diagram of LLC series resonant converter

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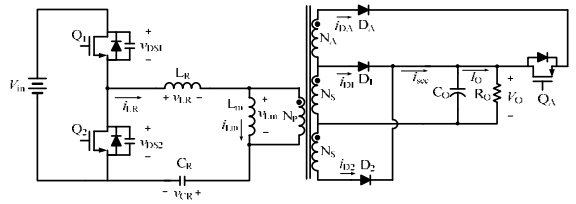


Fig 3: Circuit diagram of proposed converter

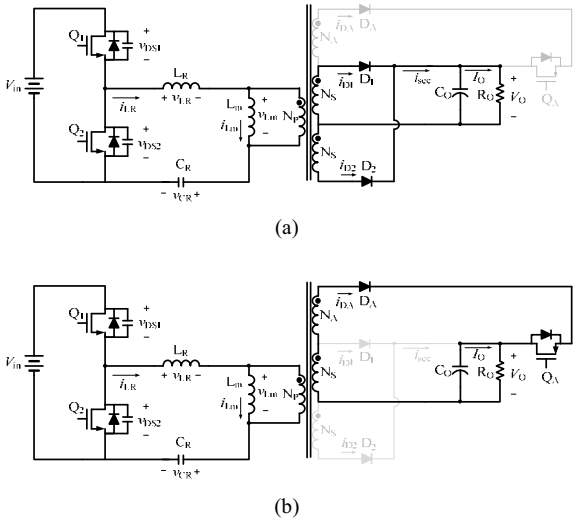


Fig 4: Operational mode (a) normal mode (b) hold-up mode

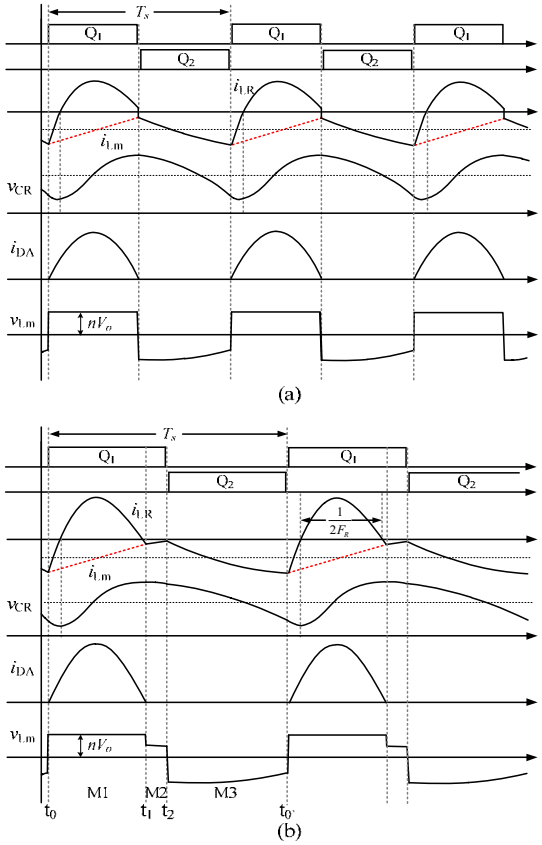


Fig 5: Key waveforms (a) Sub-above region (b) Sub-below region

secondary side of transformer is studied [1],[6], but these circuits need many components and the complexity of transformer winding is relatively high.

This paper proposes LLC series resonant converter with auxiliary circuit on transformer secondary side for hold-up time compensation. By using auxiliary hold-up time compensation circuit, the LLC converter gets higher gain when the hold-up is required and the efficiency of the converter can be improved by the optimal design. In this paper the operational principles and comparison between conventional and proposed converter are presented. To confirm the validity of the proposed circuit, the experimental results with laboratory prototype will be given.

II. PROPOSED HOLD-UP TIME COMPENSATION CIRCUIT

A. Circuit Description

Fig. 3 shows the circuit diagram of the proposed converter. The proposed circuit is identical to the conventional LLC series resonant converter except for auxiliary transformer winding (N_A), auxiliary diodes (D_A) and switch (Q_A) on the transformer secondary side. When the input voltage is nominal range, the operation of the proposed converter is the same with that of conventional one as shown in Fig. 4 (a). After AC line is off, input voltage of DC/DC converter decreases linearly. When the input voltage declines under the minimum voltage of the nominal range, the auxiliary switch is turned on to satisfy the hold-up time requirements as shown in Fig. 4 (b). As the auxiliary switch is turned on, the secondary diodes (D_1, D_2) is turned off due to reverse bias, and the powering current flows through the auxiliary diodes (D_A) only. According to the result of mode change, effective turns-ratio of transformer is changed for different condition, and the proposed converter can obtain higher dc gain by changed turns-ratio.

B. Operational Principle

In the proposed converter, the output voltage can be regulated by changing the switching frequency in common with conventional LLC resonant converter. As switching frequency is changed, the operation regions can be divided into two regions: sub-above region and sub-below region. These regions are distinct from above and below regions of the conventional LLC resonant converter because the inflection point of two regions is not resonant frequency ($F_R = 1/(2\pi\sqrt{L_R C_R})$). Fig 5 (a) and (b) show the key operational waveforms of two regions respectively. Since the operations of two regions are similar except for mode 2 of sub-below region, operation of sub-below region is explained only. The operation mode can be simply divided into three steps.

• **Mode 1 [t_0~t_1]:** When Q_2 is turned off and Q_1 is turned on at t_0, Mode 1 is started. In this mode, the difference between the resonant inductor current (i_{LR}) and the magnetizing current (i_{Lm}) is transferred to the secondary side as shown in Fig.5 (b). Resonant inductor current (i_{LR}), the magnetizing current (i_{Lm}) and the voltage across resonant capacitor (v_{CR}) can be expressed as follows:

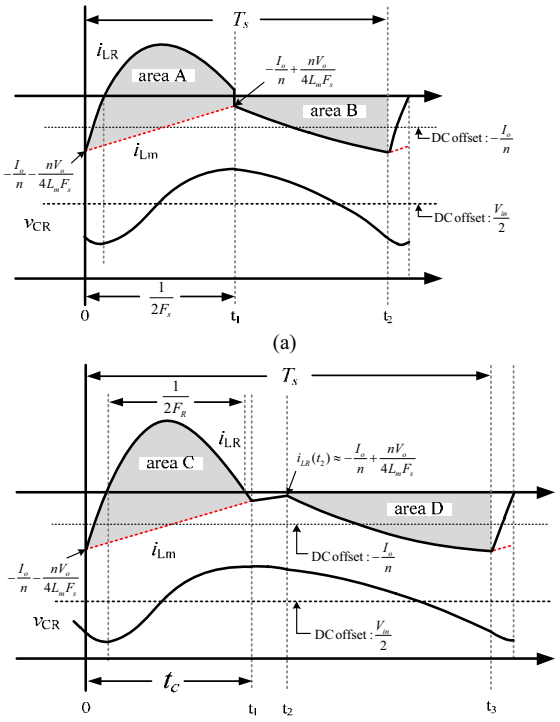


Fig 6: Current and voltage waveform of resonant tank
(a) sub-above region (b) sub-below region

$$i_{LR}(t)=\frac{V_{in}-v_{CR}(t_0)-nV_o}{Z_R}\sin\omega_R(t-t_0)+i_{LR}(t_0)\cos\omega_R(t-t_0) \quad (1)$$

$$i_{Lm}(t)=i_{LR}(t_0)+\frac{nV_o}{L_m}(t-t_0) \quad (2)$$

$$v_{CR}(t)=v_{CR}(t_0)\cos\omega_R t+(V_{in}-nV_o)\left(1-\cos\omega_R(t-t_0)\right)+i_{LR}(t_0)Z_R\sin\omega_R(t-t_0) \quad (3)$$

$$where,\ n=\frac{N_P}{N_S},\quad \omega_R=\frac{1}{\sqrt{L_RC_R}},\quad Z_R=\sqrt{\frac{L_R}{C_R}}$$

• **Mode 2 [t_1~t_2]:** When the resonant current (i_{LR}) is equal to the magnetizing current (i_{Lm}), mode 2 begins. At this mode, the output voltage is not reflected to primary side of transformer because secondary side diode blocks the negative current. Therefore, a series resonant condition is changed as follows:

$$i_{LR}(t)=i_{Lm}(t)=\frac{V_{in}-v_{CR}(t_1)}{Z_m}\sin\omega_m(t-t_1)+i_{LR}(t_1)\cos\omega_m(t-t_1) \quad (4)$$

$$v_{CR}(t)=v_{CR}(t_1)\cos\omega_m(t-t_1)+V_{in}\left(1-\cos\omega_m(t-t_1)\right)+i_{LR}(t_1)Z_m\sin\omega_m(t-t_1) \quad (5)$$

$$where,\quad \omega_m=\frac{1}{\sqrt{(L_m+L_R)C_R}},\quad Z_m=\sqrt{\frac{L_m+L_R}{C_R}}$$

• **Mode 3 [t_2~t_0']:** Mode 3 begins when switch Q_2 is turned on at t_2. The current and voltage of resonant tank is respectively decreased as following equations:

$$i_{LR}(t)=i_{Lm}(t)=\frac{v_{CR}(t_2)}{Z_m}\sin\omega_m(t-t_2)+i_{LR}(t_2)\cos\omega_m(t-t_2) \quad (6)$$

$$v_{CR}(t)=v_{CR}(t_2)\cos\omega_m(t-t_2)+i_{LR}(t_2)Z_m\sin\omega_m(t-t_2) \quad (7)$$

C. DC Voltage Gain

For the comparison of voltage gain between proposed converter and LLC converter, the precise voltage gain of the proposed converter is required.

• **Sub-above region:** DC voltage gain can be obtained from area A as shown in Fig. 6(a) because the difference between the resonant inductor current (i_{LR}) and the magnetizing current (i_{Lm}) is transferred to the secondary side. The equation can be expressed as follow:

$$I_o=\frac{n\times(area\ A)}{T_s}=\frac{1}{T_s}\int_0^{1/2F_s}n\left(i_{LR}(t)-i_{Lm}(t)\right)dt \quad (8)$$

The offset current of magnetizing inductor can be calculated by current-sec balance of resonant capacitor and the initial value of i_{LR} can be obtained from the slope of i_{Lm} as follow:

$$i_{LR}(0)=i_{Lm\_offset}-\frac{\Delta i_{Lm}}{2}=-\frac{I_o}{n}-\frac{nV_o}{4L_mF_s} \quad (9)$$

Since the resonant capacitor acts as a DC blocking capacitor, the DC offset of v_{cr} is half of the input voltage. The initial value of v_{cr} can be calculated from the area B of Fig. 6 as follow:

$$v_{CR}(0)\approx\frac{V_{in}}{2}-\frac{[Area\ B]}{2C_R}=\frac{V_{in}}{2}-\frac{1-\cos\left(\pi F_m/F_S\right)}{\omega_m\sin\left(\pi F_m/F_S\right)}\frac{V_o}{nR_oC_R} \quad (10)$$

From equation (1), (2), (8), (9) and (10), the DC voltage gain can be obtained as follows:

$$\frac{V_o}{V_{in}}=\frac{1}{2n\left(1+\frac{Z_RN}{4L_mF_SM}\right)+\frac{1}{nR_oC_R}\left(\frac{1}{M}\left(\frac{1}{F_S}+\frac{N}{\pi F_R}\right)-A\right)} \quad (11)$$

where, $M=\sin(\pi F_R/F_S),\quad N=1-\cos(\pi F_R/F_S)$

$$A=\frac{1-\cos\left(\pi F_m/F_S\right)}{\omega_m\sin\left(\pi F_m/F_S\right)}$$

• **Sub-below region:** In this region, it assumed that the current slope of i_{Lm} at mode 2 is nearly the same with that of mode 1. Therefore, the initial values of i_{LR} and v_{CR} are equal to equation (9) and (10) respectively. DC voltage gain of sub-below region also can be obtained from area C as shown in Fig. 6 (b) as follow:

$$I_o=\frac{n\times(area\ C)}{T_s}=\frac{1}{T_s}\int_0^{t_c}n\left(i_{LR}(t)-i_{Lm}(t)\right)dt \quad (12)$$

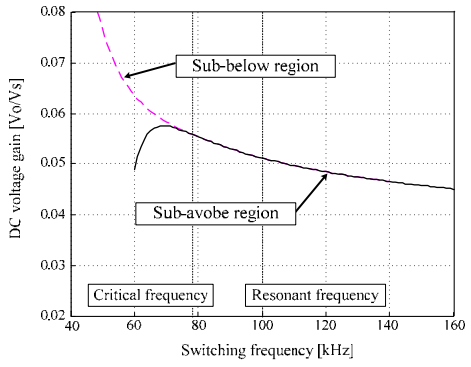
From equation (1), (2), (9), (10) and (12), the DC voltage gain can be obtained as follows:

$$\frac{V_o}{V_{in}}=\frac{1}{2n\left(1+\frac{Z_RN}{4L_mF_SM}\right)+\frac{1}{nR_oC_R}\left(\frac{1}{M}\left(\frac{2}{F_S}+\frac{N}{\pi F_R}\right)-A\right)-\frac{n}{L_mC_RM}\left(\frac{t_c}{2F_S}-t_c^2\right)} \quad (13)$$

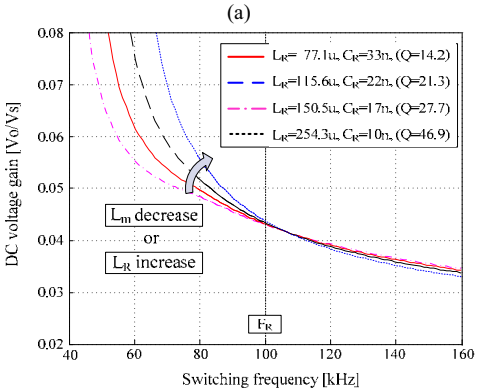
However, the conduction time (t_c) as shown in Fig. 6(b) is varied according to the initial values of current and voltage of resonant tank. The conduction time can be found from equation (1), (2) as follow:

$$i_{Lm}(t_c)=i_{LR}(t_c) \quad (14)$$

$$i_{LR}(0)+\frac{nV_o}{L_m}t_c=\frac{V_{in}-v_{CR}(0)-nV}{Z_R}\sin\omega_R(t_c)+i_{LR}(0)\cos\omega_R(t_c) \quad (15)$$



(a)



(b)

Fig 7: DC voltage gain at hold-up time compensation mode

From the equation (9), (10), (13) and (15), the graph of DC voltage gain can be depicted as shown in Fig. 7.

Fig. 7 (a) shows the two graph of sub-below and sub-above mode. As mentioned before, the critical point of two regions is far from resonant frequency. Fig 7 (b) shows DC voltage gain of the proposed converter with varying Q factor. DC voltage gain characteristic of the proposed converter is similar to that of conventional one as shown in Fig. 7 (b).

III. Comparison between Conventional and Proposed Converter

When AC line is off, the link voltage linearly is decreased. Fig. 8 shows the minimum voltage of link capacitor after hold-up time (ex: 20ms) according to the link capacitance. As link capacitance is larger, the LLC resonant converter has the smaller input voltage range. However, because the volume of link capacitor is increased as link capacitance increases as shown in Fig. 8, size of link capacitor has to be limited for high power density. Therefore, the LLC resonant converter has to cover the wide input voltage range for high power density.

Fig. 9 (a), (b) shows the required switching frequency versus varied input voltage for LLC converter, which is obtained by the fundamental element simplification (FES) [4]-[13] and the voltage gain can be represented by

$$G_{DC}=\frac{V_o}{V_s}=\frac{1}{2n\sqrt{\left\{1+\frac{1}{k}\left[1-\left(\frac{F_R}{F_S}\right)^2\right]\right\}^2+\left[\left(\frac{F_S}{F_R}-\frac{F_R}{F_S}\right)\frac{\pi^2}{8n^2}Q\right]^2}} \quad (16)$$

$$where,\ n=\frac{N_P}{N_S},\quad F_R=\frac{1}{2\pi\sqrt{L_RC_R}},\quad Q=\sqrt{\frac{L_R}{C_R}}\frac{1}{R_O},\quad k=\frac{L_m}{L_R}$$

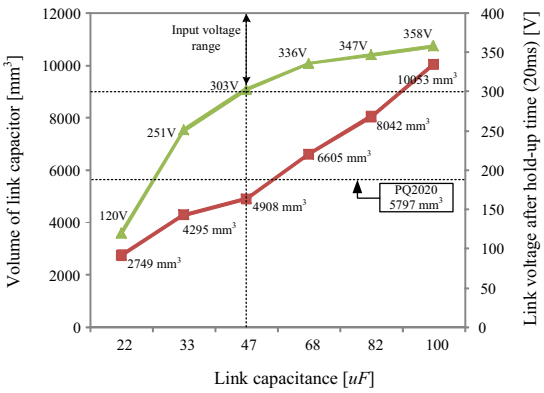
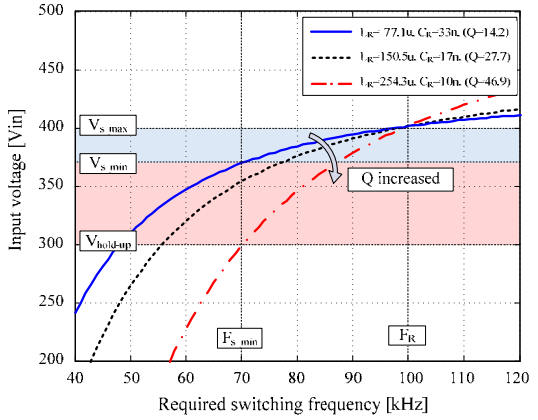
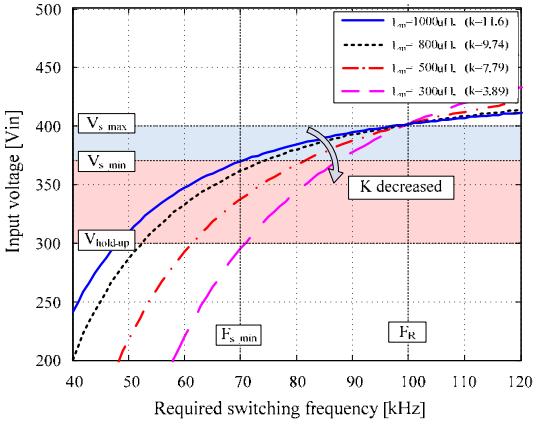


Fig 8: Volume of link capacitor and minimum link voltage after hold-up time (20ms)



(a)



(b)

Fig 9: Required switching frequency versus input voltage (a) according to L_R, (b) according to L_m

Due to wide input voltage range, the higher dc gain is required for output voltage regulation. In conventional LLC resonant converter, the switching frequency of the converter is changed to the lower frequency to regulate the output voltage for higher gain to meet hold-up time requirements. However, lower switching frequency makes magnetizing elements larger and the efficiency becomes lower due to large transformer. Therefore, the limitation of switching frequency (F_{s_min}) is required to ensure the high power density. For small switching frequency variation, higher resonant inductance (L_R) is needed for higher gain as shown in Fig. 9 (a). But a large

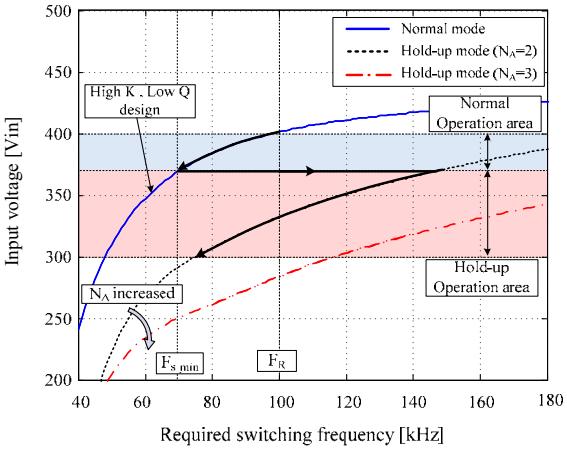


Fig 10: Gain characteristic of proposed converter

inductor core is needed for high L_R and the power density and efficiency also gets lower. In case low L_R is selected for small size of resonant inductor, the higher gain can be also got by reducing the magnetizing inductance (L_m) as shown in Fig. 9 (b). Nevertheless, small L_m causes the high RMS current of the primary switches and it lowers overall efficiency of the converter. In brief, for small switching frequency variation, the low k design (high L_R and low L_m) is required, but it has a bad influence on power density and efficiency.

However, the proposed converter with auxiliary hold-up time compensation circuit can be optimally designed with high k at the normal operation condition regardless of hold-up time. When the input voltage decreases under minimum input voltage, hold-up operation mode is started. Fig. 10 shows the gain characteristic of the proposed converter. The solid line of Fig. 10 is the gain of LLC converter with high k design regardless of hold-up time. In hold-up time mode, the graph of voltage gain is changed to dashed line of Fig. 10. The switching frequency does not exceed F_{s_min} for higher gain by changed hold-up mode as shown in Fig. 10, and thus the converter can be designed optimally regardless of hold-up time requirements. Therefore, proposed circuit extends the power density and conversion efficiency at nominal input voltage.

IV. Experimental Results

To confirm the validity of proposed converter, prototype with 80W and 16.5V output has been built. Table I summarizes the components list of the proposed converter. The resonant frequency is designed as 100 kHz. Fig. 12 shows the key experimental waveforms of the proposed circuit when the input voltage maintains nominal level (370V~400V) and drops to minimum input voltage (300V) under the full load condition. As can be shown in these figures, when the input voltage maintains nominal level, switching frequency of the proposed circuit is changed from F_R (100 kHz) to F_{s_min} (70 kHz) as input voltage variation. When the input voltage decreases to the minimum input voltage, the auxiliary switch is turned on as shown in Fig. 11, and the hold-up time compensation circuit is operated as shown in Fig. 12 (c).

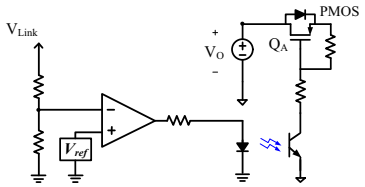
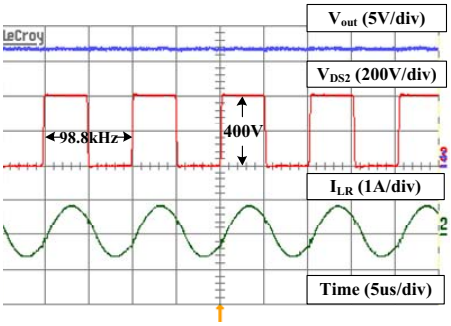
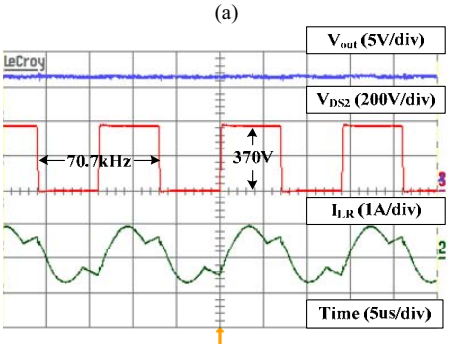


Fig 11: Circuit diagram of proposed converter



(a)



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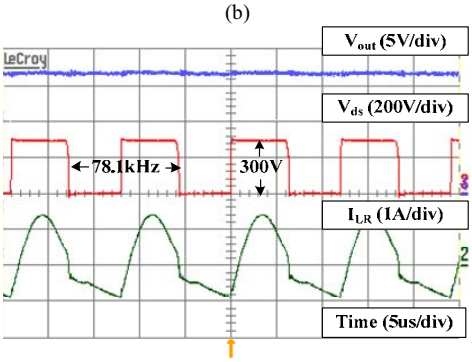
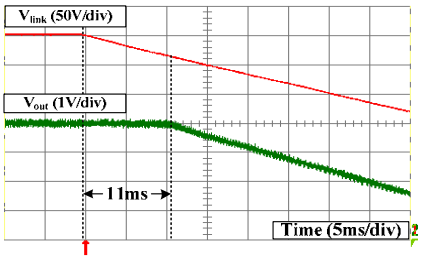


(c)

Fig 12: Key wave forms (a) When link voltage is 400V, (b) When link voltage is 360V, (c) When link voltage is 300V

TABLE I.
COMPONENTS LIST OF PROPOSED CONVERTER

Link capacitance	47uF
Primary switches(Q_1,Q_2)	IPA50R299CP
Secondary didoes (D_1,D_2,D_A)	SBR30A45CT
Resonant capacitance (C_R)	33 nF
Resonant inductance(L_R)	77 uH
Transformer	PQ2620
Magnetizing inductance (L_m)	1mH
Transformer turns ratio (N_P,N_S,N_A)	47 : 4 : 2
Output capacitance (C_o)	780 uF
Controller	L6599 (T_{dead}=300ns)



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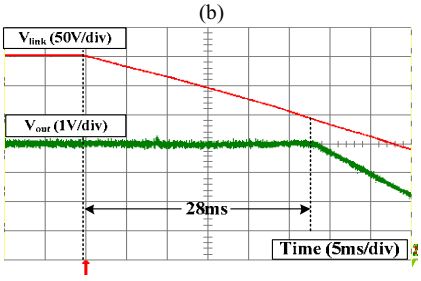

(c)

Fig 13: Hold-up time waveforms of prototype
(a) without auxiliary circuit, (b) with auxiliary circuit

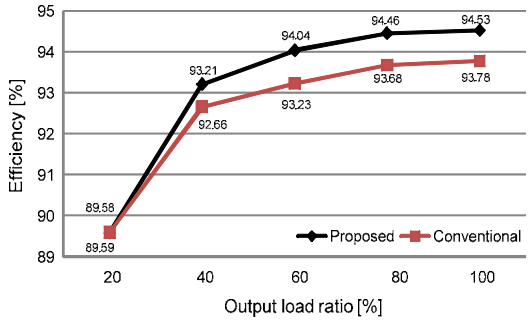

Fig 14: Efficiency comparison between conventional and proposed converter

Fig. 13 shows the hold-up time waveform when link voltage is decreased. The hold-up time of output voltage V_o is about 11ms under full load condition without auxiliary hold-up time compensation circuit as shown Fig. 13 (a). When the prototype works with the proposed auxiliary circuit properly, the measured hold-up time is extended to 28ms as shown Fig. 13 (b).

Fig.8 shows the measured efficiency for different load conditions. As expected, the efficiency of the proposed converter is higher than that of conventional converter because the proposed converter can be optimally designed with low L_R and high L_m (high k design).

V. Conclusions

To satisfy the hold-up time specification, the wide input range design is required, but it deteriorates the power density and efficiency. To solve hold-up time problems, in this paper, the LLC series resonant converter with auxiliary hold-up time compensation circuit is proposed. By using proposed hold-up time compensation circuit, the LLC converter gets higher gain when the hold-up is required and the efficiency of the converter can be improved by the optimal design in the nominal input voltage level. The validity of the proposed converter was also verified through experimental results with 80W and 16.5V adapter prototype.

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