Impact of interfacial layer control using \( \text{Gd}_2\text{O}_3 \) in \( \text{HfO}_2 \) gate dielectric on GaAs

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(Received 6 February 2007; accepted 30 March 2007; published online 2 May 2007)

Structural and electrical properties of \( \text{HfO}_2 \) and \( \text{HfO}_2/\text{Gd}_2\text{O}_3 \) gate stacks on \( p \)-GaAs substrates have been investigated. It has been demonstrated that the presence of thin layer of \( \text{Gd}_2\text{O}_3 \) between \( \text{HfO}_2 \) and GaAs improves metal-oxide-semiconductor device characteristics such as interface state density, accumulation capacitance, frequency dispersion, and leakage current. It is also found that \( \text{HfO}_2/\text{Gd}_2\text{O}_3 \) stack can reduce the interfacial GaAs-oxide formation, thus reduce the outdiffusion of elemental Ga and As during post-thermal annealing process. Such suppression of outdiffusion significantly improves the electrical properties of the dielectric stacks. © 2007 American Institute of Physics. [DOI: 10.1063/1.2732821]

Metal-oxide-semiconductor (MOS) field-effect transistors on GaAs would offer a number of advantages over Si-based devices. The six times higher electron mobility of GaAs compared to that of Si makes GaAs an attractive candidate for future complementary MOS (CMOS) devices and higher breakdown fields would support high-power/temperature applications.\(^1\)–\(^5\) However, there is a critical obstacle to GaAs MOS devices, which is the lack of stable and high-quality insulators on GaAs that can match the performance of SiO\(_2\) on Si.\(^6\)

Much progress has been made to form a high-quality gate dielectric on III–V semiconductor.\(^7\)–\(^13\) Recently, hafnium oxide (\( \text{HfO}_2 \)), as one of the promising high-\( K \) dielectric candidates for high mobility Si CMOS devices, has demonstrated good electrical characteristics on GaAs.\(^14\)–\(^16\) However, there is large frequency dispersion, hysteresis voltage, and low effective mobility for \( \text{HfO}_2/\text{GaAs} \) gate stacks.\(^15\),\(^16\) Therefore, in order to successfully integrate this dielectric into GaAs CMOS technology, there are a few important issues to be addressed, including degradation in interface property and thermal stability. One approach to overcome these obstacles is using multimetal oxides, incorporating another metal, such as Mg, Ti, Al, and Cr, into hafnium-based dielectric to reduce interfacial layer growth on GaAs.\(^17\) Gadolinium oxide (\( \text{Gd}_2\text{O}_3 \)) is one of the few binary metal oxides which is a very promising candidate for GaAs surface passivation.\(^1\),\(^13\)\(^17\) However, multimetal oxide with \( \text{Gd}_2\text{O}_3 \) and \( \text{HfO}_2 \) has not been reported yet. In this letter, we present the electrical and structural and characterization of \( \text{HfO}_2/\text{Gd}_2\text{O}_3 \) gate stacks, in comparison with \( \text{HfO}_2 \), on \( S \)-passivated \( p \)-GaAs.

MOS capacitors were fabricated on \( p \)-GaAs (100) wafers. These wafers were uniformly Zn doped with a carrier density of \( \sim 1 \times 10^{16} \text{ cm}^{-3} \). The samples in this work have used HCl cleaning for 1 min for the removal of surface oxide, followed by \( \text{(NH}_3)_2\text{S} \) last cleaning for 3 min for \( S \) passivation of GaAs surface. The 7 nm thick \( \text{HfO}_2 \) dielectric layers were deposited at room temperature by sputtering using \( \text{HfO}_2 \) target and 80 W rf power in an Ar ambient at 3 mTorr. For some wafers, a thin layer of \( \text{Gd}_2\text{O}_3 \) (2 nm) was deposited using sputter, prior to \( \text{HfO}_2 \) deposition. Postdeposition annealing (PDA) was carried out in a \( N_2 \) ambient at 500 °C for 1 min by rapid thermal annealing. The interfacial microstructure was observed by high-resolution transmission electron microscope (HRTEM), TaN metal, deposited by sputtering, was used for gate electrode.

Figure 1(a) shows the \( C-V \) characteristics of GaAs MOS capacitors with \( \text{HfO}_2 \) and \( \text{HfO}_2/\text{Gd}_2\text{O}_3 \) gate dielectrics, measured at a frequency of 100 kHz. The improved \( C-V \) shape can be observed for \( \text{HfO}_2/\text{Gd}_2\text{O}_3 \) gate stacks. It is evident that the \( \text{HfO}_2/\text{Gd}_2\text{O}_3 \) stack capacitor shows a higher maximum accumulation capacitance \( (C_{\text{ox}}) \) of 75 pF compared to the single \( \text{HfO}_2 \) capacitor. Figures 1(b) and 1(c) show the HRTEM image of \( \text{HfO}_2 \) and \( \text{HfO}_2/\text{Gd}_2\text{O}_3 \) gate stacks on \( p \)-GaAs substrates, respectively. The physical thicknesses of \( \text{HfO}_2 \) and \( \text{Gd}_2\text{O}_3 \) are 7.4 and 1.6 nm, respectively, as measured from TEM images. Although the physical thickness for \( \text{HfO}_2/\text{Gd}_2\text{O}_3 \) stack is thicker than the single \( \text{HfO}_2 \), \( C_{\text{ox}} \) is higher for \( \text{HfO}_2/\text{Gd}_2\text{O}_3 \) stack than single \( \text{HfO}_2 \). This result indicates that the thin gadolinium oxide layer on GaAs efficiently decreases the formation of GaAs oxides and suppresses the low-\( K \) interfacial layer regrowth, and thus leads to the large accumulation capacitance.\(^17\),\(^18\) The flatband voltages of \( \text{HfO}_2 \) and \( \text{HfO}_2/\text{Gd}_2\text{O}_3 \) are \( -1.3 \) and \( -0.7 \) V, respectively. The large negative flatband voltage indicates the presence of positive fixed charges in the \( \text{HfO}_2 \) film, which may be due to the oxygen vacancy/out diffusion of Ga and As. Therefore, the less negative shift of the \( C-V \) curve for \( \text{HfO}_2/\text{Gd}_2\text{O}_3 \) can be explained as a result of the reduction of the positive charges in the oxide which may be attributed less outdiffusion of elemental Ga and As in the oxides. The hys-
teresis voltage for HfO2 dielectric deposited on p-GaAs is 300 mV, while that for HfO2/Gd2O3 stack is 200 mV.

The C-V curves measured at frequencies of 10, 20, 40, 100, and 200 kHz for HfO2 and HfO2/Gd2O3 dielectrics show the frequency dispersions in accumulation and depletion regions, as shown in Fig. 2. The amounts of frequency dispersions in accumulation capacitance, evaluated as $\Delta C_{ox}$, are 18% and 8.5% for HfO2 and HfO2/Gd2O3 samples, respectively. The frequency dispersion in accumulation is attributed to the formation of an inhomogeneous layer at interface between gate dielectric and substrate. From Fig. 2 it is noted that the presence of Gd2O3 between HfO2 and p-GaAs improved the frequency dispersion by reduced interfacial layer formation. The amounts of frequency dispersion in the depletion region, evaluated as the change of voltage $V_{FB}$ at flatband between 200 and 10 kHz, are 600 and 240 mV for HfO2 and HfO2/Gd2O3 dielectrics, respectively. As the frequency dispersion in the depletion region is mainly due to the presence of interfacial traps, the result indicates that the presence of Gd2O3 reduces the interface trap density, too. Our separate evaluation of interface trap densities, measured from the combination of single-frequency C-V and G-V characteristics using Hill’s method has also shown the same trend. The expression used for calculating the interface trap density is given by

$$D_{it} = \frac{(2/\alpha qA)(G_{max}/\omega)}{[(G_{max}/\omega C_{ox})^2 + (1 - C_m/C_{ox})^2]^2},$$

where $G_{max}$ is the maximum conductance in the G-V plot with its corresponding capacitance ($C_m$), $C_{ox}$ is the oxide capacitance, $\omega$ is the angular frequency, and $A$ is the gate area of the capacitor. The interface densities are $7 \times 10^{12}$ and $4 \times 10^{12}$ eV$^{-1}$ cm$^{-2}$ for HfO2 and HfO2/Gd2O3 gate stacks, respectively. Figure 3 shows the leakage current characteristics of the HfO2 and HfO2/Gd2O3 stacks on p-GaAs substrates. The large decrease of the leakage current at low bias ($V_g = -1$ V) for the HfO2/Gd2O3 stacks is attributed to the improved interfacial layer formation and reduced defects inside the gate dielectric.

In order to understand the improvement mechanism of the interface quality in HfO2/Gd2O3/p-GaAs stack, thin films of HfO2 (2 nm) and HfO2/Gd2O3 (2 nm/1 nm) gate stacks were prepared and analyzed by x-ray photoelectron spectroscopy (XPS). Figure 4(a) shows typical XPS spectra of the Hf 4f peaks for HfO2 gate dielectrics deposited on p-GaAs substrates. The spectra collected for Hf 4f can be...
The Gibbs free energy of formation per O atom is $-544 \text{ kJ/mole}$ (Ref. 14) for HfO$_2$, which is less negative than the Ga and As oxides. Therefore, it may be responsible for large GaAs$_2$O$_5$ oxides at the interface for HfO$_2$ on GaAs.

In conclusion, it has been demonstrated that the insertion of Gd$_2$O$_3$ into HfO$_2$ on GaAs gate stack is an effective way of improvement of interface quality. Even though the overall physical thickness is increased due to the additional layer, the total equivalent oxide thickness is decreased due to the suppression of low-K interfacial layer growth. Other electrical properties such as frequency dispersion, hysteresis, and leakage current are all improved when Gd$_2$O$_3$ layer is inserted to the interface. Therefore, it is concluded that the Gd$_2$O$_3$ is an excellent material for interface passivation when Hf-based high-K dielectric is used on GaAs substrate for high speed CMOS application.

The HfO$_2$/Gd$_2$O$_3$ gate stack deposited on p-GaAs and annealed at 500 °C for 1 min in N$_2$ ambient. (a) Hf 4f and (b) As 3d spectra for HfO$_2$. (c) Hf 4f and (d) As 3d spectra for HfO$_2$/Gd$_2$O$_3$ gate stacks. Spectra were recorded using Al Kα radiation and a take-off angle of 30°.

![Figure 4](https://example.com/figure4.png)

**FIG. 4.** (Color online) XPS spectra for thin HfO$_2$ and HfO$_2$/Gd$_2$O$_3$ gate stacks deposited on p-GaAs and annealed at 500 °C for 1 min in N$_2$ ambient. (a) Hf 4f and (b) As 3d spectra for HfO$_2$. (c) Hf 4f and (d) As 3d spectra for HfO$_2$/Gd$_2$O$_3$ gate stacks. Spectra were recorded using Al Kα radiation and a take-off angle of 30°.

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