A novel energy-recovery circuit for a plasma display panel (PDP) is proposed in this paper. Two different ERCs, ERC-Y and ERC-X, are used for both sides of the PDP, and the slow falling and fast rising times can be employed. The ERC-Y discharging $C_p$ to zero employs the slow falling time and is composed of an LC resonant circuit biased by $0.5V_s$, which reduces the conduction loss and a voltage drop across a parasitic resistance, and decreases a current stress. The ERC-X charging $C_p$ to $V_s$ employs the fast rising time and is composed of an LC resonant circuit biased by $V_s$, which ensures the stable light emission, fully charges $C_p$ to $V_s$ regardless of a parasitic resistance, and compensates for a large gas-discharge current. Therefore, it features the zero voltage switching (ZVS), low electromagnetic interference (EMI), low current stress, no severe voltage notch, and high energy-recovery capability. The operation of the proposed circuit and design considerations are discussed in detail, and experimental results are presented to show the validity of the proposed circuit.

II. Introduction

Since the PDP has advantages such as the wide view angle, lightness, thinness, high contrast, and large screen, it is one of the most leading candidates for large screen TVs. Since the PDP is composed of sustaining (X) and scanning (Y) electrodes covered by a dielectric and MgO layers, it can be equivalently regarded as a capacitance load $C_p$. In order to generate a gas-discharge in the PDP, a sustaining voltage is alternately applied across between X and Y electrodes using a full bridge inverter. Therefore, there exists considerable energy loss of $2C_pV_s^2$ in a parasitic resistance per each cycle without ERC. Furthermore, an excessive surge current during charging and discharging intervals of the PDP increases the current rating of switches, and causes severe electromagnetic interference (EMI) noise and heat problems [1-4].

To solve these problems, several approaches have been proposed. Among them, the prior circuit I using an LC resonant circuit biased by $0.5V_s$ shown in Fig. 1(a) features the low conduction loss and high performance [5]. However, the voltage drop caused by a parasitic resistance prevents the PDP from being fully charged and discharged to $V_s$ and zero, respectively, which results in the serious hard switching, excessive surge current, serious power dissipation, severe EMI noise, and poor energy-recovery capability. In particular, the voltage drop caused by a parasitic resistance is increased, as the rising time is faster. Therefore, the faster rising time to ensure the stable light emission increases the power dissipation due to a hard switching in this circuit. Moreover, a large gas-discharge current causes a serious voltage notch across the PDP.

Since the gas-discharge generally occurs immediately after $C_p$ is charged to $V_s$, the fast rising time, that is, the fast charging time, of the PDP is required to ensure the stable light emission, i.e., below about 400 nsec. On the other hand, since the falling time, that is, the discharging time, of the PDP does not affect the gas-discharge characteristics, it is neither important nor critical to the light emission. However, the falling time is equal to the rising time in prior circuit I, and the faster rising time makes a resonant inductor smaller, resulting in a higher resonant current. Therefore, it has a disadvantage that the peak current of resonant inductor discharging the PDP is inevitably increased.  

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**Fig. 1. Prior ERCs.**

(a) Prior circuit I

(b) Prior circuit II
The prior circuit II using an LC resonant circuit biased by \( V_s \) shown in Fig. 1(b) features good energy-recovery performance [6]. The PDP is fully charged and discharged to \( V_s \) and zero, respectively, in spite of a voltage drop caused by a parasitic resistance. Also, the inductor current compensates the large gas-discharge current, which results in no severe voltage notch and the reduced current stress on main switches. However, it still has disadvantage that an excessive conduction loss occurs due to a very large inductor current fed back to an input voltage source without any energy-recovery action just after the PDP is discharged to zero. Moreover, since the falling time is equal to the rising time in this circuit like prior circuit I, the peak current of resonant inductor discharging the PDP is inevitably increased.

To overcome these drawbacks of prior circuits, a novel ERC for the PDP shown in Fig. 2(a) is proposed in this paper. Two different ERCs are used for both sides of the PDP, and the slow falling and fast rising times are employed in the proposed circuit. The ERC-Y discharging \( C_p \) to zero employs the slow falling time and is composed of an LC resonant circuit biased by \( 0.5V_s \), reducing a conduction loss like prior circuit I. The slow falling time reduces a voltage drop across a parasitic resistance so that the hard switching of \( M_1 \) and \( M_3 \), power dissipation, surge current, and EMI noise are not serious in the proposed circuit. Also, it makes the peak current of \( L_1 \) lower than that of \( L_2 \), resulting in a lower current stress on ERC-Y compared with ERC-X. The ERC-X charging \( C_p \) to \( V_s \) employs the fast rising time and is composed of an LC resonant circuit biased by \( V_s \). Thus, it helps to ensure the stable light emission, fully charge \( C_p \) to \( V_s \), regardless of a parasitic resistance, achieve the ZVS of \( M_2 \) and \( M_4 \), and reduce the EMI noise. Furthermore, since it compensates for a large gas-discharge current, there is no severe voltage notch. Also, this gas-discharge compensation can reduce the current stress on \( M_2 \) and \( M_4 \). Therefore, the proposed circuit features the high energy-recovery capability.

II. Operation of the proposed circuit

Fig. 2(b) shows key waveforms of the proposed circuit. One cycle operation is divided into six modes. It is assumed that \( C_1 \), \( C_2 \), \( C_3 \), and \( C_4 \) are equal to \( C_{oss} \), and \( V_{Ca} \) is equal to \( 0.5V_s \). Fig. 3 shows the equivalent circuits and voltage across the PDP in mode 1 and 3.

Mode 1 (t0~t1): When \( M_4 \) and \( M_5 \) are turned off, and \( M_1 \) and \( M_6 \) are turned on at \( t_0 \), mode 1 begins. \( L_2 \) begins to charge \( C_p \) and discharge \( C_2 \) with initial conditions of \( v_{Cp}(t_0)=0 \) and \( i_{L2}(t_0)=0 \) in this mode, and the equivalent circuit of this mode is formed as shown in Fig. 3(a). Therefore, the following equations are obtained from this figure.

\[
V_{Cp}(t) = V_s \left[ 1 - e^{-(t-t_0)/(\pi/\omega_{l1})} \right] \left( \cos \omega (t-t_0) + \frac{1}{\omega} \sin \omega (t-t_0) \right)
\]  

(1)
where $\tau = 2L_2/R_{\text{par}}$, $\omega = [1/(L_2(C_p + 2C_{\text{oss}}))]^{-1/2} 0.5$, and $R_{\text{par}} = \text{parasitic resistance.}$

As shown in Fig. 3(a), $V_{C_p}$ is charged by an LC resonance biased by $V_s$. Thus, as shown in Fig. 3(c), the PDP is fully charged to $V_s$ in spite of a parasitic resistance. As well, the rising time $t_1-t_0$ can be faster without any hard switching according to decreasing $L_2$. Therefore, $M_2$ can be turned on under the ZVS, and $C_p$ is fully charged to $V_s$ with the fast rising time in spite of a parasitic resistance. After a quarter resonant cycle, $V_{C_p}$ is clamped on $V_s$, the gas-discharge begins to take place, and $i_{L_2}$ freewheels through $D_2$ and $M_6$.

Mode 2($t_1-t_2$): When $M_2$ is turned on and $M_6$ is turned off at $t_1$, mode 2 begins. In this mode, since $i_{L_2}$ fed back to an input voltage source through $M_2$ and $d_{x_1}$ compensates a large part of the gas-discharge current through $M_2$, the current stress on $M_2$ can be considerably reduced as well as the severe voltage notch across the PDP can be effectively overcome.

Mode 3($t_2-t_3$): When $i_{C_p}$ becomes zero at $t_2$, $M_1$ is turned off, $M_7$ is turned on, and mode 3 begins. $L_1$ begins to discharge $C_p$ and $C_3$, and charge $C_1$ with initial conditions of $v_{C_p}(t_2) = V_s$, $i_{L_2}(t_2) = 0A$ in this mode, and the equivalent circuit of this mode is formed as shown in Fig. 3(b). Therefore, the following equations are obtained from this figure.

$$v_{C_p}(t) = \frac{V}{2} \left[ 1 + e^{-\omega(t-t_0)/\tau} \left( \cos \omega(t-t_0) + \frac{1}{\omega \tau} \sin \omega(t-t_0) \right) \right]$$

$$i_{L_1}(t) = -\frac{V}{2}\frac{e^{-\omega(t-t_0)/\tau}}{\tau} \sin \omega(t-t_0)$$

where $\omega = [1/(L_1(C_p + 2C_{\text{oss}}))]^{-1/2} 0.5$.

As shown in Fig. 3(b), since the PDP is discharged by an LC resonance biased by $V_s/2$, there exists the hard switching due to a parasitic resistance. However, as shown in Fig. 3(c), $L_1$ increases according to increasing the falling time $t_2-t_3$, so that the peak current of $L_1$ and the voltage drop, $V_d(1-e^{-\omega(t)/\tau})/2$, across a parasitic resistance are considerably reduced, which results in discharging $C_p$ to 0V without a severe hard switching and reducing the current stress on ERC-Y. Therefore, the proposed circuit features no severe hard switching, less power dissipation, and low surge current due to the gas-discharge current compensation and slow falling time. Furthermore, it shows low EMI noise levels, and high energy-recovery capability.

The next circuit operation of $t_3-t_6$ is similar to that of $t_0-t_3$.

### III. Design considerations

The voltage across the PDP is charged from 0 to $V_s$ during the time interval $t_0-t_1$, and discharged from $V_s$ to 0 during the time interval $t_2-t_3$. Thus, if parasitic components are neglected, $L_1$ and $L_2$ can be determined from equations (1) and (3) as follows:

$$L_1 = \frac{1}{C_p + 2C_{\text{oss}}} \left( \frac{t_1-t_0}{\tau} \right)^2$$

$$L_2 = \frac{4}{C_p + 2C_{\text{oss}}} \left( \frac{t_2-t_0}{\tau} \right)^2$$

Since the brightness of a PDP depends on the operational frequency and rising time, the rising time $t_1-t_0$ is required to be as fast as possible. However, since this brightness is irrelevant to the falling time $t_2-t_3$, it is good for this time to be as slow as possible under the given operational frequency in order to reduce the current stress on ERC-Y and parasitic voltage drop.

### IV. Experiment results

To verify the behavior and analysis of the proposed circuit, a prototype circuit is implemented with specifications of $f_s = 200kHz$, $C_p = 2nF$ (6-inch PDP), $L_1 = 49\mu H$, $L_2 = 26\mu H$, rising time $= 400ns$, falling time $= 1100ns$, $V_s = 145V$, and $M_1-M_8 = 2SK2995$. Fig. 4 shows the experimental results of the proposed circuit displaying the white image. From Fig.
Cp is fully charged to Vs without hard switching due to the LC resonance biased by Vs, and discharged to 0 V without severe hard switching due to the slow falling time. Also, the current stress on ERC-Y is considerably reduced compared with ERC-X due to the slow falling time. Moreover, since \( i_{L2} \) compensates for the large amount of the gas-discharge current, the current stress on M2 and M4 and the voltage notch are effectively reduced. From Fig. 4(b), M2 and M3 are turned on under the ZVS without severe hard switching due to the LC resonance biased by Vs and the slow falling time, respectively. Fig. 5 shows the power consumption with respect to the applied sustaining voltage. The proposed circuit has the lower power consumption than the prior circuit in Fig. 1(b) due to ERC-Y biased by 0.5Vs and the slow falling time.

### V. Conclusions

A novel ERC for the PDP having the slow falling and fast rising times has been proposed in this paper. The ERC-Y biased by 0.5Vs with the slow falling time reduces a conduction loss, and the ERC-X biased by Vs helps to fully charge \( C_p \) to Vs with the fast rising time in spite of a parasitic resistance. The slow falling time makes the current stress on ERC-Y lower than that on ERC-X and \( C_p \) discharged to zero without severe hard switching. Furthermore, there is no severe voltage notch due to the gas-discharge current compensation. The proposed circuit features the low EMI and high energy-recovery capability. Therefore, it is expected to be suitable for the PDP.

### References


