20 GHz Integrated CMOS Frequency Sources with a Quadrature VCO using Transformers

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***Abstract* — A fully integrated 20 GHz frequency source is implemented with a VCO and a doubler in 0.18 um CMOS process. A 10 GHz quadrature voltage controlled oscillator (QVCO) is implemented using transformer-coupled resonator. The VCO can be tuned between 10.2 and 11.4 GHz and has low phase noise of -118.67 dBc/Hz at 1 MHz offset frequency with 1.8 V power supply. The Figure of merit (FOM) is 188 dB. The 20 GHz differential signal is generated by harmonics of quadrature signals of the VCO with a balanced frequency doubler. To increase output power of harmonics, a pinch-off clipping is used without any buffers and DC level shifter, since the proposed VCO has RF signals with low DC level. The frequency multiplier of which output can be tuned between 19.8 and 22 GHz has low noise of -111.67 dBc/Hz at 1 MHz offset frequency. The phase noise of the multiplier is 7 dB higher than that of the VCO. The output power is -6.83 dBm and the VCO output power is -6 dBm.**

***Index Terms* — quadrature, VCO, transformer, frequency doubler, CMOS, pinch-off clipping.**

I. INTRODUCTION

The fully integrated CMOS millimeter-wave frequency sources have been paid great attention due to its low cost and the integrability with other analog and digital circuits although Si substrate has higher loss than GaAs substrate. Recently the phase noises of CMOS VCOs in X-band are comparable to these of GaAs [1]. Above X-band, it is difficult to design a CMOS VCO with good performance. One suitable approach is a frequency doubling. There are, therefore, several reasons to use a lower frequency oscillator and a doubler instead of oscillator at high frequency. The phase noise added by the doubler is usually less than what an oscillator at the higher frequency would give. Furthermore, in a high frequency phase-locked loop oscillator, it is difficult to realize a frequency divider at the desired output frequency. Therefore, in an oscillator with a doubler, the divider can work only at the half of the output frequency [2].

Several MMIC-based millimeter-wave frequency doubler have been realized and reported in the literature, they can be made a single ended or a balanced [3][4]. Balanced operation can offer broadband suppression of the input frequency. However, the power consumption and chip size is more than doubled compared to single ended topologys. The quadrature signals can generate a pair of differential signals at 2×f0 by balanced doubling. To has the high quality signal of the doubler, the accurate quadrature signals with low phase noise are needed.

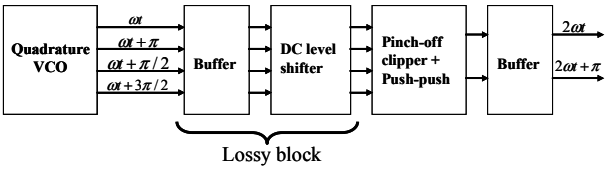

Fig. 1. Block diagram of a frequency doubler with a VCO

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A simple method to get the accurate quadrature signals is coupling of two symmetric LC-tank VCOs to each other. This is implemented successfully under X-band. However, above X-band, this had not been reported in CMOS integrated circuits due to poor property of integrated inductors. Although a distributed VCO (DVCO) is one of attractive solutions in CMOS process, it demands larger area than a VCO with LC-tank. To improve the Q-factor of an integrated inductor in CMOS process, a transformer is used in a QVCO [1]. Two coupled LC-tank with a transformer can improve Q-factor of a resonator. Moreover, the transformer separates gate biases of series-connected transistors from cross-coupled RF signals [1]. Owing to this property, the current source in the propose VCO can be removed while the VCO maintains low noise under low power supply [5]. Furthermore, the VCO allows RF output port with low DC bias. This is useful when the VCO is connected to a frequency doubler.

In section II, we explain the topology and noise reduction mechanism of the proposed transformer-based QVCO and the frequency doubler. In section III, the measurement results are presented.

II. CIRCUIT DESIGN

Fig. 1 shows the block diagram of a balanced frequency boubler with a quadrature VCO. The pinch-off clipper and push-push block is used to increase power of harmonics [4]. The input of pinch-off clipper needs lower DC level while the DC level of a VCO output is equal to power

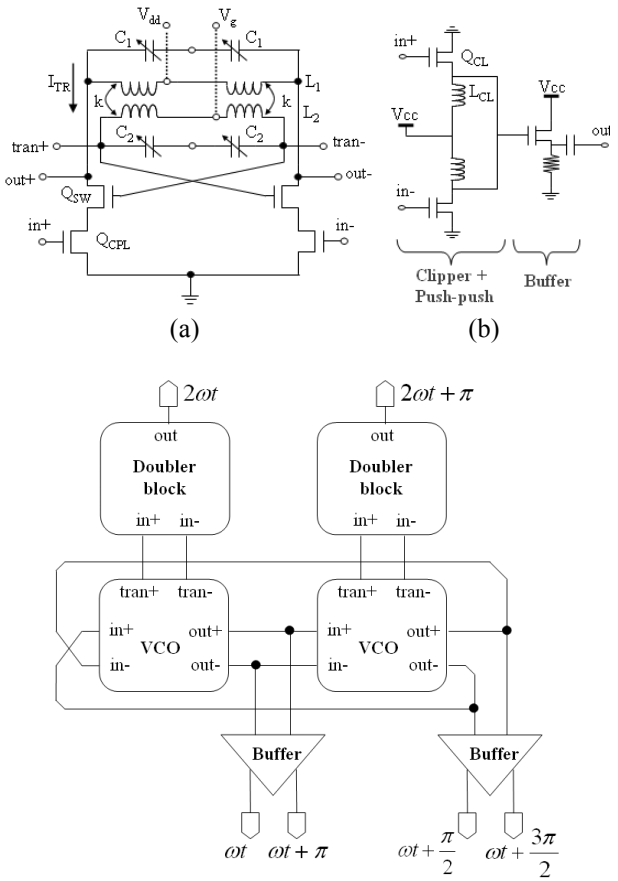

Fig. 2. (a) Schematic of the proposed transformer-based VCO core (b) the doubler block to generate differential 2×f0 signal. (c) Block diagram of the proposed frequency source with the doubler and the proposed QVCO

supply voltage or half of that in a conventional VCO. Thus, DC level shifter is needed. However, the DC level shifter and a buffer are lossy blocks. Low loss buffer in CMOS process needs large current which causes the degradation of the phase noise.

The proposed QVCO has two output pairs since it have transformer-based resonator in each VCO block. One is out± with DC level of V_{dd} and the other is tran± with DC level of Vg as shown in Fig. 2(a). Since the minimum point of phase noise is Vg = 0.6 V, tran± can be connected to the pinch-off clipper directly. Fig. 2(b) shows the frequency doubler to generate differential 2×f0 signal. It is composed of two clipping transistors, two inductor-loads and one source follower. The follower can be replaced with 2nd harmonics matching networks to get more high power of 2nd harmonics. But, the follower is identical with buffers of the QVCO to compare the VCO outputs. The output of the clipper has large even and small odd

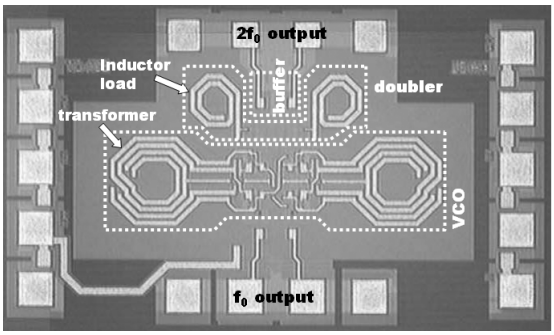

Fig. 3. Photograph of the proposed frequency source with the doubler and proposed QVCO (1280×760 μm2)

harmonics except fundamental. Thus, odd harmonics is not important. Since 2nd harmonics is larger than 4th one, the 4th harmonics is not considerable generally. The block diagrams of the frequency source with the doubler and the proposed VCO are presented in Fig. 2(c), which can get integrated millimeter-wave signal above 20 GHz in CMOS process due to the simple and lossless structure.

Generally, a differential VCO uses a current source to start up reliably and to prevent large output swing from increasing phase noise. On the other hand, a VCO without a current source can operate under low power supply. The current source in the proposed QVCO can be removed while the VCO maintains low noise under low power supply due to the characteristics of a transformer and series-connected transistors [5].

Q_{CPL} serves as a current source in the proposed VCO. Although Q_{CPL} in the triode region is not good as a current source, phase noise is improved owing to the absence of noises from a current source. The QVCO without a current source can operate under lower power supply than a VCO with a current source, while phase noise is not degraded. Furthermore, the QVCO provides RF output with low DC bias.

V_g can tune gate of Q_{SW} without changing V_{CC} though L_2. Although V_g connected to only gate of Q_{SW}, the bias of Q_{CPL} is more sensitive than that of Q_{SW} for V_g variations. Gain, current, and noise of Q_{CPL} are decreased as V_g is decreased.

III. Experimental Results

The presented integrated frequency source with the doubler and the proposed QVCO is implemented using 0.18 μm CMOS process, which provides 5 layers for interconnection and 2 μm thick top analog metal. Fig. 3 shows the photograph of the fabricated multipliers. The chip sizes is 1280×760 μm2 including the bonding pads.

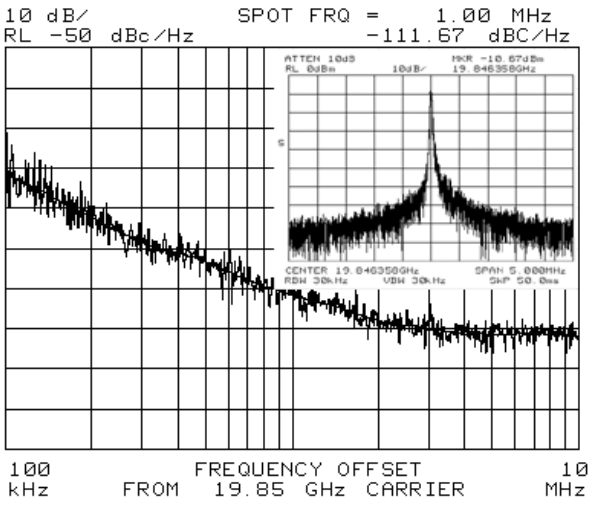

Fig. 4. Output spectrum of the douber at the center frequency of 19.85 GHz and phase noise measurement at an offset frequency range 100 kHz to 1 MHz at the center frequency (-111.67 dBc/Hz at 1 MHz offset frequency)

The source is composed of the proposed QVCO, frequency, a doubler and a buffer. The buffer is identical with the buffer of the VCO to compare harmonics variation. The inductor load is connected to drain of the pinch-off clipper. The spiral inductor is used for the load, since the inductor for a load does not need high Q-factor at 2fo frequency.

The frequency source was carried out with on-wafer probing. The output spectrums and the phase noise performance were obtained from HP8564E spectrum analyzer and its phase noise measurement kit. The cable loss including a probe tip in measurement setup is about 2 and 3.5 dB at 10 and 20 GHz respectively. Fig.4 shows the measured output spectrums and phase noises of the doubler at the center frequency of 19.85 GHz. The phase noise performance under the supply bias of 1.8 V is -111.5 dBc/Hz at 1 MHz offset frequency, which is 7 dB higher than that of the QVCO. The phase noise is increased by 6 dB theoretically when the output frequency is doubled [6]. 1 dB degradation maybe caused by noise of clippers and substrate noise.

Fig. 5 shows the harmonics powers of the VCO and the doubler. The 2nd harmonics of the VCO is about 10 dB lower than the fundamental. However, the 2nd harmonic of the doubler is 10 67 dB higher than the fundamental at maximum point. 3rd and 4th harmonics are below -25 dBm in both outputs. The DC bias of the VCO core's output port and the buffer is supply voltage. Thus the buffer has the strong nonlinearity, which increases harmonics power. The difference of fundamental and 2nd harmonics is 6 dB higher in the VCO core than that in the

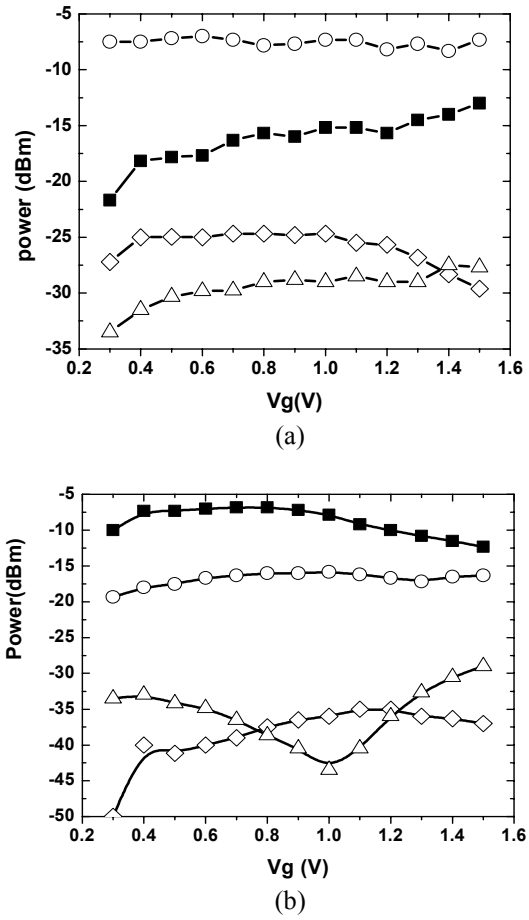

Fig. 5. The output power of harmonics vs. the gate voltage (a) the output of the VCO (b) the output of the doubler. (○ 1st harmonics ■ 2nd harmonics ◊ 3rd harmonics Δ 4th harmonics)

buffer as the simulation of Agilent ADS. Thus, the doubler gain of about 20 dB is expected.

Vg is the gate bias of Q_{SW} in the VCO and Q_{CL}. The fundamental harmonics of the VCO is almost constant. On the other hand, the 2nd harmonics of the multiplier is increased and fundamental is decreased as Vg is decreased. Fig, 5 (b) shows that increase of the 2nd until Vg = 0.4 V. The decrease at Vg = 0.3 is caused by the property of the VCO core as shown in Fig. 5 (a).

The tuning ranges are 1.58 and 2.17 GHz with the 0 ~ 1.5 V and -1.5 ~ 1.5 V. The tuning range is 2 times of the QVCO's tuning range. The measurement results are summarized in Table I. As shown in Fig. 6, the phase noise and FOM are better and comparable to ever reported CMOS VCOs.

TABLE I
COMPARISON OF QVCO AND DOUBLER

	QVCO	Doubler
Osc. Freq. (GHz) (tuning range)	10.18 ~ 11.37 (1.19 GHz)	19.84~22.01 (2.17 GHz)
phase noise @ 1 MHz offset	-118.67 dBc/Hz	-111.67 dBc/Hz
Output Power	-6 dBm	-6.83 dBm
Bias	1.8 V, 6.57 mA	1.8 V, 22.4 mA
FOM	188 dB	181.5 dB

IV. CONCLUSION

A fully integrated 20 GHz frequency source is presented with 0.18 um CMOS process, which has low noise of -111.67 dBc/Hz at 1 MHz offset. The source is composed of a frequency doubler and the proposed QVCO, which has low phase noise of -118.67 dBc/Hz at 1 MHz offset frequency under 1.8 V power supply. The VCO has the FOM of 188 dB, which is the best value among X-band VCOs. To increase output power of the doubler, a pinch-off clipping is used without any buffers and DC level shifter, since the proposed VCO has RF signals with low DC level owing to the transformer. The phase noise of the doubler is 7 dB higher than that of the VCO. The output power is -6.83 dBm and the VCO output power is -6 dBm. This millimeter-wave frequency source is suitable to a PLL in a low ft CMOS process since the source has low phase noise and provides signals at the half frequency of the output.

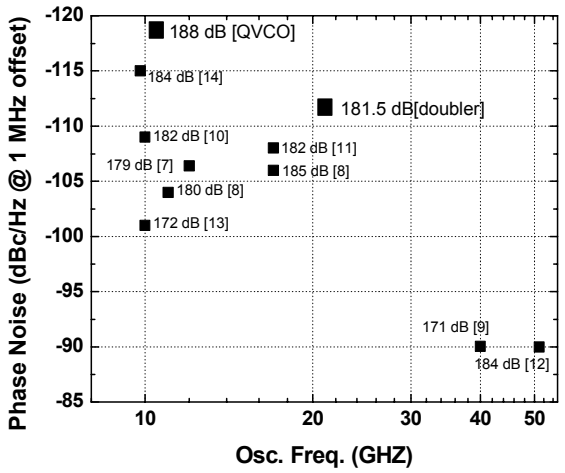

Fig. 6. Phase noise comparison to recently published CMOS VCO's, operating in the 9~51 GHz range. (FOM at 1 MHz offset frequency [reference])

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