A V-band VCO and frequency divider MMICs for phase-locked loop

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Abstract — This paper presents a VCO with frequency doubler and a 1/8 frequency divider MMICs for a V-band PLL using cost effective InGaP/GaAs HBT Technology. The VCO was implemented common base inductive topology with 27.5 GHz differential outputs and 55 GHz doubler output. The 1/8 frequency divider was implemented by connecting two stages of static frequency divider circuits after dynamic one. To achieve higher operating frequency, active loads are used in the dynamic frequency divider. The maximum operating frequency of the 1/8 frequency divider is higher than \(f_T/2\) of transistor.

Index Terms — Frequency divider, voltage-controlled oscillator (VCO), phase-locked loop (PLL), frequency doubler and InGaP/GaAs HBT.

I. INTRODUCTION

The increasing demands of millimeter wave wireless communication and radar systems raise the need of low cost millimeter wave sources. InGaP/GaAs HBTS have somewhat lower \(f_T\) and \(f_{MAX}\) than GaAs pHEMTs or InP based transistors. However, these HBTS are very attractive to be used for millimeter wave application due to their low 1/f noise, reliable fabrication process and lower manufacturing cost.

To implement phase-locked loop (PLL), a voltage-controlled oscillator (VCO) and a frequency divider are key parts. The operating frequency of VCO and frequency divider has been increased for higher frequency PLL. Several developments of VCO and frequency divider have been reported [1-2].

This paper presents a VCO with frequency doubler and 1/8 frequency divider MMICs for V-band PLL using cost effective InGaP/GaAs Technology.

II. CIRCUIT DESIGN

Fig. 1 shows a block diagram of PLL. In this work, a VCO with frequency doubler and a 1/8 frequency divider were realized for higher frequency PLL. The block diagram of the 1/8 frequency divider and the balanced VCO with differential amplifiers and the frequency doubler are also shown in Fig. 1. Two differential amplifiers have two differential output pairs, which drive the 1/8 frequency divider and the frequency doubler. The 1/8 frequency divider is composed of a dynamic...
A. Voltage Controlled Oscillator

Fig. 2 shows the schematic of the balanced VCO circuit, which used common base inductive feedback topology [3]. It consists of microstrip line resonators (MLR1, MLR2) and a pair of common base inductive feedback negative resistance cells (Q1, Q2). The oscillation frequency is determined by \( \lambda/4 \) microstrip line resonators (MLR1, MLR2). The core current is controlled by current mirror. The base-collector junction capacitance of HBT is used as a varactor for the frequency tuning.

B. Differential amplifiers and frequency doubler

Fig. 3 shows the schematic of the differential amplifiers. Two differential output pairs are needed to drive the frequency divider and the frequency doubler. Each of the differential amplifiers has just one input port connected to the VCO. This circuit contains a pair of emitter follower stages and output differential amplifier. Emitter follower is used as a buffer to isolate the VCO from external perturbations.

The frequency doubler is accomplished by setting the bias of the class B mode. This stage generates as much power at the second harmonic as possible and consumes low dc currents [4].

C. Dynamic frequency divider

A 1/8 frequency divider was implemented by connecting two stages of static frequency divider and an output buffer after the dynamic one. Fig. 4 shows the schematic of the dynamic frequency divider, which is based on the principle of regenerative frequency division [5]. The dynamic frequency divider consists of a mixer, a...
low-pass filter and an amplifier. The input signal is applied to a mixer, which is followed by a low-pass filter and an amplifier. The output signal is fed back to the other mixer input. The maximum operating frequency of the dynamic divider is mainly determined by the loop’s cutoff frequency. To achieve higher operating frequency, using active loads make it possible to increase the loop’s cutoff frequency without degrading gain [6].

D. Static frequency divider

The static frequency divider composed of master-slave D-flip-flop, which is made of emitter coupled logic. The operating frequency of ECL logic is higher than that of the CML logic despite of large power consumption. Fig. 5 shows the schematic of master-slave D-flip-flops. The static frequency dividers are used in the second and third stages of the 1/8 frequency divider.

III. EXPERIMENT RESULTS

The VCO with frequency doubler chip size is $1.95 \times 0.9 \text{ mm}^2$ as shown in Fig. 6. The output spectrums and the phase noise performance of the fundamental oscillation frequency of 27.5 GHz were obtained from HP8564E spectrum analyzer. The losses of the microprobe, the cable and the connectors are about 5 dB at 27.5 GHz. 55 GHz output spectrum of the frequency doubler was measured using HP E4407B with HP 1194V (50~75 GHz) harmonic mixer. The losses of probe tip and waveguide components in V-band measurement setup are about 3.4 dBm at 55 GHz. Fig. 7 shows the output spectrum and the phase noise of the fundamental oscillation frequency. The phase noise is -88.5 dBc/Hz at 1 MHz offset frequency at the fundamental oscillation frequency of 27.7 GHz. Fig. 8 illustrates the fundamental oscillation frequency and the output power characteristic as varying the varactor control bias from 0 V to 5 V. It provides the peak output power of
-1 dBm. Fig. 9 shows the measured 2\textsuperscript{nd} harmonic output frequency of 55.3 GHz with a tuning range of 1.4 GHz. Output power is -22 dBm and phase noise is -75.5 dBc/Hz at 1 MHz offset frequency at the 2\textsuperscript{nd} harmonic frequency.

The 1/8 frequency divider chip size is 2.05 x 0.9 mm\textsuperscript{2} as shown in Fig. 10. One of 1/8 differential output signals produced a trigger signal for Agilent 86100A oscilloscope. The input was also sampled by a directional coupler, and the waveform was monitored. The input and output waveforms at maximum operating frequency (f\textsubscript{m}=28 GHz) are shown in Fig. 11 (a). The operating frequency range was 9 GHz–28 GHz. The 1/8 frequency divider was realized using InGaP/GaAs HBT technology with f\textsubscript{T} of 50 GHz and an f\textsubscript{MAX} of 120 GHz. The maximum operating frequency is higher than f\textsubscript{T}/2 of transistor.

IV. CONCLUSIONS

We present a VCO with frequency doubler and 1/8 frequency divider for V-Band PLL using cost effective InGaP/GaAs Technology. The VCO has 27.5 GHz differential outputs and 55 GHz doubler output. The 1/8 frequency divider was implemented by dynamic divider and two stages of static frequency divider. The 1/8 frequency divider operates up to 28 GHz, which is higher than f\textsubscript{T}/2 of transistor. To our knowledge the operating frequency of 55 GHz is the highest value reported for the integrated VCO and frequency divider using InGaP/GaAs HBT Technology up to now.

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