Thermal Characteristics of InGaP/GaAs HBT Ballasted with Extended Ledge

Sanghoon Jeon, Hyun-Min Park, and Songcheol Hong

Abstract—A InGaP/GaAs heterojunction bipolar transistor structure is proposed in which the base epitaxial layer underneath the extended ledge works as a base ballast resistor. The structure eliminates the critical alignment for a passivation ledge formation as well as additional process steps for external base ballast resistor. Both ballasted and unballasted devices were fabricated and compared. Small signal equivalent circuit gives us the magnitude of the effective ballast resistance. The thermal characteristics, including gain-collapse and S-factor loci, were measured, which is alternative to collapse loci [1]. We applied the extended ledges to InGaP/GaAs HBTs [11]. Fig. 1 shows the layout of the proposed device, which has the passivation ledge of 2 μm. The epitaxial base resistance is used as the base ballast resistor instead of an external NiCr resistor, which, we expect, improves process yield. The thermal instability can be incorporated to ensure the reliability [5]–[7]. Thus, the spacing between an emitter mesa and a base electrode is always introduced to some extent. Extended ledges allow a well-passivated extrinsic base region and easy fabrication process, while it degrades high speed performances due to the increase of base resistances. Technology has been pushed to the direction to make small ledges for better high speed performance, although an external ballast resistor must be added in power applications. Here, we proposed a device structure, in which the extended passivation ledge can work as a ballast resistor.

HBTs based on the InGaP/GaAs material system have received considerable interest as active devices in high power amplifiers [8]–[10]. Since InGaP/GaAs HBTs can be fabricated with highly selective etchants, improved yields and homogeneities are expected in comparison to AlGaAs/GaAs HBTs [11]. Fig. 1 shows the layout of the proposed device, which has the passivation ledge of 2 μm. The epitaxial base resistance is used as the base ballast resistor instead of an external NiCr resistor, which, we expect, improves process yield. The epitaxial resistor also has a temperature dependence. The positive temperature coefficient of GaAs resistivity results in resistance changes with temperature variations. This means that the ballasting effect is enhanced with the increase in temperature and counterbalances the negative resistance of the device.

In this paper, we describe the thermal and microwave characteristics of an extended ledge ballasted (ELB) InGaP/GaAs HBTs in comparison to conventional self-aligned HBTs. In addition, we investigate the temperature dependency of base epiresistance. The epitaxial structure and the fabrication process are described in Chapter II. Compared characteristics between ELB and self-aligned HBTs appear in Chapter III. Chapter IV includes the models for ELB HBT and discussions. Finally, the conclusion is followed in Chapter V.

I. INTRODUCTION

Heterojunction bipolar transistor (HBT) has been used in microwave high power amplifiers. As in Si BJT, it exhibits thermal instability-related failures when operated under large dc or RF drive conditions [1]–[3]. This instability is due to the negative temperature coefficient of emitter-base turn-on voltages and the strong electrothermal positive feedback with high thermal resistance. The thermal instability can be reduced by use of a ballast resistor in series with each emitter or base [2], [3] or by thermal shunt techniques [4]. On the other hand, it is well known that a passivation ledge around an emitter periphery must be incorporated to ensure the reliability [5]–[7]. Thus, the spacing between an emitter mesa and a base electrode is always introduced to some extent. Extended ledges allow a well-passivated extrinsic base region and easy fabrication process, while it degrades high speed performances due to the increase of base resistances. Technology has been pushed to the direction to make small ledges for better high speed performance, although an external ballast resistor must be added in power applications. Here, we proposed a device structure, in which the extended passivation ledge can work as a ballast resistor.

HBTs based on the InGaP/GaAs material system have received considerable interest as active devices in high power amplifiers [8]–[10]. Since InGaP/GaAs HBTs can be fabricated with highly selective etchants, improved yields and homogeneities are expected in comparison to AlGaAs/GaAs HBTs [11]. Fig. 1 shows the layout of the proposed device, which has the passivation ledge of 2 μm. The epitaxial base resistance is used as the base ballast resistor instead of an external NiCr resistor, which, we expect, improves process yield. The epitaxial resistor also has a temperature dependence. The positive temperature coefficient of GaAs resistivity results in resistance changes with temperature variations. This means that the ballasting effect is enhanced with the increase in temperature and counterbalances the negative resistance of the device.

In this paper, we describe the thermal and microwave characteristics of an extended ledge ballasted (ELB) InGaP/GaAs HBTs in comparison to conventional self-aligned HBTs. In addition, we investigate the temperature dependency of base epiresistance. The epitaxial structure and the fabrication process are described in Chapter II. Compared characteristics between ELB and self-aligned HBTs appear in Chapter III. Chapter IV includes the models for ELB HBT and discussions. Finally, the conclusion is followed in Chapter V.

II. THE EPITAXIAL STRUCTURE AND FABRICATION

The epitaxial structure for this work consists of a 5000 Å GaAs subcollector (n = 5 x 10¹⁸ cm⁻³), a 7000 Å GaAs collector (n = 5 x 10¹⁶ cm⁻³), a 1000 Å GaAs base (p = 3 x 10¹⁸ cm⁻³), a 500 Å InGaP emitter (n = 5 x 10¹⁷ cm⁻³), a 1500 Å GaAs emitter cap (n = 4 x 10²⁸ cm⁻³), a 500 Å grade from GaAs to In₀.₅₀Ga₀.₅₀As, and a 500 Å In₀.₅₀Ga₀.₅₀As contact layer (n = 1 x 10¹⁸ cm⁻³). A Ti/Pt/Au emitter contact is first deposited and used to mask the emitter etch. The InGaAs contacting layer and GaAs emitter cap are etched in citric acid, which stops on the InGaP emitter, and the InGaP emitter is then selectively etched in an HCl based etch. Low resistance Ti/Pt/Au base contacts are deposited and subcollector etched. After mesa-isolating the device, AuGe/Ni/Au collector contacts are deposited. Polyimide is used for planarization and devices are contacted for probing by a Ti/Au metallization and a 2.5 μm plated bridge.

III. DEVICE CHARACTERISTICS

In order to examine the thermal stability, Vᵦᵣᵦ₁ regression characteristics of ELB HBTs were measured, which is alternative to collapse loci and S-factor loci [1]. We applied the Vᵦᵣᵦ₁ device as inputs and measured Iᵦ₁ and Vᵦᵦ₁ as Iᵦᵦ₁ increased, then obtained Fig. 2. For comparison, the regression characteristics of self aligned HBTs is also shown. Both are one-finger devices, which have the emitter area of 3 x 20 μm² and belong to the same batch. As the power dissipation increases and junction temperature increases, a smaller base-emitter voltage is required to have a certain Iᵦ₁. Therefore, Vᵦᵦ₁ decreases with the further increase of Iᵦ₁. Such a Vᵦᵦ₁ regression characteristic was known to be a main cause of thermal instability. Consequently, the collapse of current gain occurs at the bias condition where ∂Iᵦ₁/∂Vᵦᵦ₁ → ∞, i.e., at the regression
Fig. 2. Measured $V_{BE}$ regression plot. Both $I_C$ and $V_{BE}$ are measured as $I_B$ varies, while the input collector-emitter biases are fixed at 3, 4, 5, and 6 V.

Fig. 3. Measured $I-V$ characteristics of four-finger HBTs used for the study of thermal instability. DC current gains were 23 and 45 for the self-aligned device and ELB device, respectively. Base current level was properly adjusted in order to compare the operation of the two kinds of devices at the same power consumption. We measured four-finger devices, which have the same dimension of Fig. 2. Fig. 3 illustrates the $I-V$ characteristics of the two devices. Dashed curves represent the measured collapse loci of the self-aligned HBT and the solid curves represent the measured $I-V$ curve of ELB HBT, which has no collapse loci. Actually, we were not able to measure the high voltage region because the device has low $BV_{CEO}$ of 7 V. However, thermal stability is improved by the ballast resistor.

IV. MODELS AND DISCUSSIONS

In order to obtain the magnitude of an base ballast resistor in the ELB HBT, we extracted a transistor's small signal equivalent circuit parameters. Fig. 4 shows the small signal equivalent circuit of HBTs and Table I shows extracted parameters of a self-aligned and an ELB HBTs, respectively. The measured devices have one-finger emitter of $3 \times 20 \mu m^2$. All of the extracted parameters are almost the same in the two devices, except $R_{be}$ and $R_{ei}$. The difference of $R_{be} + R_{ei}$ corresponds to the added resistance of ELB HBT, which was $35 \Omega$. By tailoring the ledge size, one can expect that various values of a ballast resistor can be obtained. $f_t$ of 44 GHz and $f_{max}$ of 30 GHz were obtained in self-aligned device and $f_t$ of 37 GHz and $f_{max}$ of 28 GHz in ELB device. As in Fig. 5, the base-ballast resistor makes $f_{max}$ and $f_t$ to be smaller. If any kind of ballast resistor introduced, the degradations in $f_{max}$ and $f_t$ are inevitable. Thus, the magnitude of the ballast resistor must be as small as possible to have high speed, which must be determined on account of the thermal resistance $R_{th}$ of device and dissipated power.

One can utilize the positive temperature coefficient of resistors. The epitaxial base resistor under the extended ledge has a large positive temperature coefficient. The temperature rises the highest at the base resistor because this is located very near the heat sources of base-collector junction. To investigate the temperature dependence of the base resistance, the sheet resistance of TLM test pattern was measured at

![Small signal equivalent circuit of HBTs.](image)

![Fig. 5. Measured small signal maximum available gain as a function of frequency. Measured self-aligned and ELB HBTs are all one-finger, with $3 \times 20 \mu m^2$ finger area.](image)

<table>
<thead>
<tr>
<th>Small Signal Parameters</th>
<th>Self-Aligned</th>
<th>ELB</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_V$ (pF)</td>
<td>75.6</td>
<td>79.8</td>
</tr>
<tr>
<td>$R_{be}$ (Ω)</td>
<td>5.0</td>
<td>17.4</td>
</tr>
<tr>
<td>$R_{ei}$ (Ω)</td>
<td>1.0</td>
<td>24.0</td>
</tr>
<tr>
<td>$R_f$ (Ω)</td>
<td>3.0</td>
<td>3.5</td>
</tr>
<tr>
<td>$R_e$ (Ω)</td>
<td>2.0</td>
<td>2.5</td>
</tr>
<tr>
<td>$C_y$ (pF)</td>
<td>44.9</td>
<td>36.6</td>
</tr>
<tr>
<td>$r_0$ (Ω)</td>
<td>1.6</td>
<td>1.7</td>
</tr>
<tr>
<td>$R_{b}$ (kΩ)</td>
<td>139</td>
<td>150</td>
</tr>
<tr>
<td>$\alpha$</td>
<td>0.96</td>
<td>0.96</td>
</tr>
<tr>
<td>$C_m$ (pF)</td>
<td>1.30</td>
<td>1.19</td>
</tr>
<tr>
<td>$f_t$ (GHz)</td>
<td>60</td>
<td>55</td>
</tr>
<tr>
<td>$\tau$ (pS)</td>
<td>1.70</td>
<td>1.75</td>
</tr>
<tr>
<td>$C_{max}$ (pF)</td>
<td>0.50</td>
<td>1.39</td>
</tr>
</tbody>
</table>
Fig. 6. Temperature dependence of base sheet resistance.

Fig. 7. Schematic diagram of HBT model with the temperature dependent resistor model.

Fig. 8. Calculated $I-V$ characteristics of two-finger HBTs. Unballasted and NiCr resistor ballasted devices show collapse loci, but the epitaxial resistor ballasted device does not. This is due to increasing resistance as junction temperature rises.

V. Conclusion

A method to implement a ballast resistor is proposed, in which the extended ledge is used as a ballast resistor as well as passivation. This also simplifies the fabrication process. The thermal characteristics of the InGaP/GaAs HBT including $I-V$ curve, regression curve, and small signal characteristics are presented and modeled. The temperature dependency of an epitaxial resistor is actively utilized and is shown to be an effective alternative for ballasting an HBT.

Acknowledgment

The author would like to thank Dr. H. Koo and Mr. S. Cho of the Hanmirotek Corp. for their valuable suggestions and participation in the fabrication of devices.

References


Impact of a High Electric Field on the Extraction of the Generation Lifetime from the Reverse Generation Current Component of Shallow $n^+\text{-}p$-well Diodes

A. Poyai, E. Simoen, and C. Claeyss

Abstract—A procedure is proposed to extract the thermal generation lifetime ($\tau_g$) profile in the depletion region of shallow $n^+\text{-}p$-well junctions surrounded by shallow trench isolation from the generation current density. This is achieved by taking account of the electric field enhancement factor. As will be shown, a more realistic $\tau_g$ profile is obtained that better reflects the trap density profile, corresponding with the deep boron ion implantation-related extended defects.

Index Terms—Diodes, electric fields, leakage current, Schottky barriers, tunneling.

I. INTRODUCTION

The potential of a p-n junction as a tool for the assessment of the carrier lifetime and generation/recombination properties of the silicon material or its surface has been recognized since the early days of semiconductor electronics. Recently, renewed interest has led to a further refinement of junction-based techniques [1], enabling separation of the different geometrical current components. These can be split up further into physical components, i.e., a generation ($J_g$), and a diffusion ($J_d$) current density in the case of area leakage current density ($J_{dA}$), from which, respectively, the generation ($\tau_g$) and recombination lifetime ($\tau_r$), can be derived. In the former case, $\tau_g$ is usually assumed constant and calculated from

$$J_{dA} = \frac{q n_i W_A}{\tau_g}$$  \hspace{1cm} (1)

where
- $q$: elementary charge;
- $n_i$: intrinsic carrier concentration;
- $W_A$: volume depletion width.

This diode assessment is currently quite popular in the defect study of silicided shallow junctions [2], as it reveals relevant information for the development of deep submicron complementary metal–oxide semiconductor (CMOS) technologies and in particular for the optimization of source/drain junctions. The latter are fabricated in a retrograde well, which has a fairly high maximum doping density. Therefore, a high maximum electric field ($F$) exists in the depletion region of a reverse-biased $n^+\text{-}p$-well junction. Consequently, in the pre-avalanche region, the $J_{dA}$ increases at a higher rate than can be expected from a simple Shockley-Read-Hall (SRH) generation mechanism. This electric field-enhanced generation rate ($\Gamma$) of charge carriers occurs when the $F$ at the junction reaches values of about $10^5 - 10^7$ V/cm. The $\Gamma$ can be caused by several effects: the Poole-Frenkel (PF) effect [3], Schottky barrier lowering [2] or trap-assisted tunneling (TAT), and band-to-band tunneling (BBT) [4]. As a result, (1) is modified to [4]

$$J_{dA} = \frac{q n_i W_A \Gamma}{\tau_g}$$  \hspace{1cm} (2)

It is the aim of this paper to investigate the nature of the electric field enhancement of the generation current in silicided $n^+\text{-}p$-well junctions surrounded by shallow trench isolation (STI). The resulting $\tau_g$ profile will be discussed in view of recently observed deep level profiles, derived from deep level transient spectroscopy (DLTS) on the same devices [5, 6].

II. EXPERIMENTAL

Shallow $n^+\text{-}p$ diodes compatible with submicron CMOS technology have been processed on 150 mm diameter Czochralski (Cz) p-type substrates. STI was used to define the active diode regions. A retrograde p-well was obtained by a deep (200 keV, $1.2 \times 10^{13}$ cm$^{-2}$) and a shallow ($55$ keV, $1.5 \times 10^{13}$ cm$^{-2}$) boron ion implantation, followed by a dopant activation anneal (10 min, 850°C). The $n^+$ region was obtained by an arsenic ion implantation ($70$ keV, $4 \times 10^{15}$ cm$^{-2}$) and anneal (10 s, 1100°C). A junction depth of around 0.15 μm was expected. A cobalt silicide with titanium capping layer was applied. Junctions with different geometry have been studied in order to separate the current and capacitance components using the procedure reported elsewhere [7].

The $I$–$V$ characteristics of the diodes were measured at the wafer level in the dark and in a voltage range of $-5$ to $+1$ V. The bias was applied to the back p-type substrate and the current was measured at the top $n^+$ contact, which was kept at neutral ground. The capacitance-voltage ($C$–$V$) measurements have been performed at 100 kHz in order to determine the depletion width and the doping density profile.

III. RESULTS AND DISCUSSION

The $J_A$ has been separated from the total leakage current by combining different geometry diodes, as described in [7]. The $J_A$ normally consists of the $J_{dA}$, and the $J_{dA}$ [1]. $J_{dA}$ has been derived from the forward $I$–$V$ characteristic by taking the ideality factor ($m$) into account [8]. The $W_A$ has been calculated from the area capacitance ($C_A$), which has been obtained from the corrected series resistance capacitance by combining different geometry diodes. The doping profile in the p-well has been found from the derivative of the curve $1/C_A^2$ versus reverse bias. For the general case of a non uniform generation lifetime, $J_{dA}$ equals the integration of $q n_i / \tau_g(x)$ from zero to $W_A$. The $F$ has been calculated by integrating Poisson’s equation numerically using the experimental doping profile. The $F$ varies from $1.7 \times 10^5$ to $5.7 \times 10^5$ V/cm for a bias of 0 to $-5$ V. As mentioned above, the $\Gamma$ can be caused by several effects. However, the BBT contribution has been found to be important at room temperature only for $F > 7 \times 10^5$ V/cm [2], so that it can be ruled out here. Therefore, PF and TAT will be considered next.