A 2.4-GHz Sub-mW Frequency Source with Current-Reused Frequency Multiplier

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Abstract — A fully integrated 2.4 GHz low-power frequency source including a 1.2 GHz voltage-controlled oscillator (VCO) and a current-reused frequency multiplier is fabricated in 0.18-µm CMOS process. The proposed frequency source tunes from 2.22 GHz to 2.45 GHz by changing control bias from 0 V to 0.7 V, and achieves a phase noise of -115.83 dBc/Hz at 1 MHz offset from a 2.2 GHz carrier frequency while drawing only 840 µA bias current (490 µA for a 1.2 GHz VCO and 350 µA for the frequency multiplier) from the low supply voltage of 0.7 V.

Index Terms — Frequency source, VCO, Frequency multiplier, Pinch-off clipper, Current-reusing.

I. INTRODUCTION

Recently, extremely low-power single-chip receivers operating in ISM (Industrial, Scientific, and Medical) bands have drawn wide attention due to the rapidly growing markets of battery-operated disposable wireless sensor network (WSN). For most sensing applications, sensor nodes spend far more time in receiving (waiting for wake-up signal) than in transmitting (answering a request). Therefore, the receiver power consumption is the most critical issue in the design of low-power transceivers, even though the power level required in transmit mode is an order of magnitude higher. Most power-consuming components in receiver operating in the UHF ranges are LO buffer, VCO and frequency divider. Especially, as operating frequency goes higher, power consumption in the frequency divider drastically increases as well as VCO. To reduce power dissipated in the frequency divider, we would like to adopt the receiver architecture as shown in Fig. 1. In this receiver architecture, the output frequency of VCO ($f_{VCO}$) is a half of RF frequency ($f_{RF}$). And a frequency multiplier, which plays the role of LO buffer to prevent injection-locking problem, generates the two times signal frequency of input. Therefore, in the receiver using a VCO with a frequency multiplier, the frequency divider can work only at a half of the RF frequency of 2.4 GHz, resulting in great power reduction.

Note that VCO and frequency multiplier should have differential output signals to remove RF feedthrough in a mixer. However, to generate a pair of differential signals operating at 2×$f_{VCO}$, previously reported frequency multipliers require quadrature input signals or additional circuitry [1-2]. These result in the increase of power consumption in a frequency source.

In this paper, we present a 2.4 GHz frequency source using a 1.2 GHz VCO and a frequency multiplier for a sub-mW wireless sensor network receiver. The proposed current-reused frequency multiplier can generate differential output signals using only differential input signals from a half frequency VCO. As a result, the entire power consumption in the frequency source including the frequency multiplier and VCO can be significantly reduced.

In the next section, we present the circuit topology and operation principles of the proposed frequency multiplier and VCO. In section III, measurement results of the fabricated frequency source are presented. Finally, summary and conclusion will follow in section IV.

II. THE PROPOSED FREQUENCY SOURCE

A. Voltage-Controlled Oscillator (VCO)

In extremely low-power implementation of VCO, to achieve large oscillation amplitude is a key issue with as
low power consumption as possible. Therefore, it is strongly required to design the VCO with maximum oscillation amplitude under a given amount of bias current. For this, the current-reused VCO topology in [3] may be a good solution with respect to low power consumption. Because the current-reused VCO can make a narrow current pulse ($I_{\text{tank}}$) with high peak value, it can achieve larger oscillation amplitude while drawing the same average DC current [4]. To stabilize the DC bias current, we have substituted a tail current source for a degeneration resistor as shown in Fig. 2. From the simulation using Agilent ADS, the peak value of $I_{\text{tank}}$ is three times as high as the average current of $I_{\text{tail}_\text{VCO}}$.

B. The Proposed Current-Reused Frequency Multiplier

A pinch-off clipper, which is biased such that gate DC bias of MOSFET ($V_G$) is set around the threshold voltage ($V_{th}$), is widely used to increase second order harmonics for frequency doubling as shown in Fig. 3 (a) [5]. Fig. 3 (b) shows the phases of 1st and 2nd harmonics of the output signals when the input signals with different phases are applied to the nMOS pinch-off clipper. Referring to Fig. 3 (b), we can see that quadrature signals have to be applied to the nMOS pinch-off clipper to make differential output signals [2].

However, to generate quadrature signals from differential VCO output signals, additional circuits such as passive poly-phase filter or active $g_m$-C filter should be employed between VCO and frequency multiplier. But this is not desirable for low power application because passive poly-phase filter causes significant signal losses and active $g_m$-C filter substantially increases power consumption.

Fig. 4 shows the concepts of the proposed current-reused differential frequency multiplier. To generate differential 2nd harmonic outputs, we use pMOS pinch-off clipper together with nMOS one as shown in Fig. 4 (a).

Fig. 5. Circuit topology of the proposed 2.4-GHz current-reused differential frequency multiplier
2\textsuperscript{nd} harmonic output of pMOS inherently has opposite phase compared with that of nMOS irrelevant to the phase of input signals. Therefore, in the proposed frequency multiplier, we can easily generate differential 2\textsuperscript{nd} harmonics by applying in-phase or differential inputs. In addition, in order to minimize power consumption, we have stacked the pMOS pinch-off clipper above the nMOS one to reuse DC bias current and inserted a large bypass capacitor \((C_{\text{bypass}})\) between two pinch-off clippers for providing a reliable AC ground, as shown in Fig. 4 (b).

Fig. 5 shows the circuit schematic of the proposed frequency multiplier. We use a tail current source to stabilize the DC bias current. And nMOS and pMOS pinch-off clippers are self-biased as shown in Fig. 5. For reliable AC signal blocking between the gate and drain nodes, a large resistor is inserted. This self-biasing technique makes the proposed frequency multiplier more immune to the variations of power supply and DC current of \(I_{\text{tail clipper}}\) and to the device mismatch.

1\textsuperscript{st} harmonic cancellation is an important issue in frequency multiplier design because 1\textsuperscript{st} harmonic can modulate the time of zero-crossing of 2\textsuperscript{nd} harmonic signal. The modulated zero-crossing can change the duty cycles of a switching stage of mixer, resulting in an asymmetry operation of the switching transistors. To cancel out the 1\textsuperscript{st} harmonic, we have designed each pinch-off clipper which consists of a pair of transistors. And then, differential outputs of VCO \((V_{\text{IN}+}, V_{\text{IN}^-})\) are applied to each transistor as shown in Fig. 5. As a result, 1\textsuperscript{st} harmonics are fully cancelled out and 2\textsuperscript{nd} harmonics are add-up because phase difference of 1\textsuperscript{st} and 2\textsuperscript{nd} harmonics are 180° and 0°, respectively, as shown in Fig. 3.

The proposed frequency multiplier also works as a LO buffer for signal isolation between VCO and mixer. In addition, the proposed frequency multiplier can reduce LO buffer noise because LC-tank can filter out flicker noise and high frequency noise which are apart from resonance frequency [7]. Low noise LO buffer eventually helps to reduce a noise figure of mixer [8].

III. MEASUREMENT RESULTS

Microphotograph of the fabricated frequency source using a 0.18 \(\mu\)m CMOS process, which provides 2 \(\mu\)m-thick AlCu layer, is shown in Fig. 6. The chip occupies an area of 1.5 \times 0.8 mm\(^2\) including pads. The frequency source consists of a 1.2 GHz differential LC-VCO and a 2.4 GHz current-reused differential frequency multiplier. To increase Q-factor, differential octagonal-shape inductors are used in both LC-tanks. We have optimized two LC-tanks, which resonate at different frequencies of 1.2 GHz and 2.4 GHz, to tune by using only one varactor control bias. The output spectrum and phase noise are obtained from HP 8564E spectrum analyzer and its phase noise measurement kit.
The fabricated frequency source consumes 840 µA bias current (490 µA for a VCO, 350 µA for a frequency multiplier) from 0.7 V power supply. The frequency source tunes from 2.22 GHz to 2.45 GHz by changing the control bias from 0 V to 0.7 V. Fig. 7 shows harmonic spectrums of the fabricated frequency source. The output power of 2\textsuperscript{nd} harmonic amplified by frequency multiplier is about -10 dBm at 2.2 GHz, which is about 23 dB larger than that of 1\textsuperscript{st} harmonic at 1.1 GHz. This result ensures that 1\textsuperscript{st} harmonics of VCO are sufficiently cancelled out by applying differential signals to a pair of transistors shown in Fig. 5. Measured phase noise at 1 MHz offset from 2.2 GHz carrier frequency is -115.83 dBc/Hz, as shown in Fig. 8. The figure of merit (FOM) of the fabricated frequency source is 187.4 dBc/Hz, excluding power consumption of the frequency multiplier. Measurement results are summarized in Table I.

IV. CONCLUSIONS

We have proposed and demonstrated a 2.4-GHz fully integrated CMOS frequency source using a current-reused differential frequency multiplier and a 1.2 GHz VCO in order to reduce power consumption of receiver. The proposed frequency multiplier can generate differential 2\textsuperscript{nd} harmonic output signals only using differential input signals and reduce power consumption by reusing DC bias current. In addition, the proposed frequency source requires no additional power and circuitry compared with conventional one which consists of VCO and LO buffer operated at RF signal frequency, because the frequency multiplier plays a role of LO buffer. The fully integrated frequency source achieves a phase noise of -115.83 dBc/Hz at 1 MHz offset from 2.2 GHz carrier frequency with 590 µW power consumption (343 µW for a VCO and 245 µW for the frequency multiplier).

ACKNOWLEDGEMENT

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REFERENCES


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<th>Item</th>
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<td>Osc. Freq. (GHz)</td>
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<td>(tuning range)</td>
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<td>Power (µW)</td>
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<tr>
<td>Phase noise @ 1MHz offset</td>
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</tr>
<tr>
<td>FOM (dBc/Hz)</td>
<td>187.4</td>
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</table>

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