increased from zero until oscillation began. This occurred for $I_C = 40 \mu A$ with corresponding values (including transistor input resistance and capacitance) of $R_1 = 9.7 \, k\Omega$ and $C_1 = 36.9 \, pF$. The device transconductance was then $g_m = 1.5 \, mA/V$. Simulation using SPICE gave curves similar to those of Fig. 5 and predicted that the Nyquist diagram passed through $(-1/g_m, 0)$ at $\omega = \omega_1$ for $g_m = 1.2 \, mA/V$.

The bias current in the active device was then increased until oscillations would not start in the circuit. The current was then reduced until oscillations started. This occurred for $I_C = 790 \, \mu A$ with $R_1 = 2.6 \, k\Omega$ and $C_1 = 52.7 \, pF$. The device transconductance was then $30 \, mA/V$, and SPICE simulation showed a Nyquist plot similar to Fig. 5(b) which passed through $(-1/g_m, 0)$ at $\omega = \omega_2$ for $g_m = 27 \, mA/V$. The measured range of $g_m$ for oscillator start-up was thus $1.5-30 \, mA/V$ compared with a predicted range of $1.2-27 \, mA/V$. This is probably an adequate margin for bias for reliable oscillator start-up in this example, but could be modified if desired using the principles developed above.

V. CONCLUSIONS

Monolithic realizations of crystal oscillators commonly use resistive feedback elements across the crystal for active-device bias purposes. In addition to a lowering of circuit $Q$, this resistance can cause conditions of unreliable start-up in the oscillator. Computer simulation and measurements have shown that this problem is related to the relative impedance levels of shunt resistance and capacitance in the circuit.

REFERENCES


On the Thermal Isolation Applications of V-Groove Technology

YEARN-IK CHOI, CHOONG-KI KIM, AND YOUNG-SE KWON

Abstract—V-groove etching technology has been applied to the thermal isolation in an integrated circuit chip. Numerical calculation shows that V-groove structure brings about 50 percent improvement in normalized temperature when compared to the conventional planar structure.

I. INTRODUCTION

Recent advances in large-scale integration (LSI) and very large scale integration (VLSI) have offered many possibilities in mixing high-performance analog circuits with dense digital circuits and combining large high-voltage devices with small low-voltage devices. These efforts have been able to reduce the cost and physical size of electrical equipment and permit single chips to compete directly with multichip systems in such areas as A/D conversion for data control and display, automotive electronics, and telecommunications.

However, large power dissipation at driver circuitry in a single chip seems to be leading to difficult thermal problems. The dissipation-induced temperature changes across a die can easily cause performance changes far in excess of the circuit design limitations and result in thermal runaway or second breakdown or self-oscillation. In particular, it is argued that thermal feedback may be responsible for a major part of $1/f$ flicker or excess noise [1].

In this paper, we report on the possibility of utilizing V-groove etching technology for thermal isolation in an integrated circuit chip. Two specific examples are treated to show the effectiveness of the V-groove. The first is the thermal isolation of the output driver in an integrated circuit such as a multistage monolithic amplifier, and the second is a thermal
Fig. 1. Thermal model of an integrated circuit chip which has a localized heat source. Heat is generated in an active layer such as semiconductor junction.

Fig. 2. Simplified two-dimensional model of various chip morphologies. (a) Conventional planar structure, (b) V-groove isolation structure, (c) truncated V-groove structure.

under these assumptions, the time-dependent heat equations are

\[ \rho C_p \frac{\partial T}{\partial t} = k \left( \frac{\partial^2 T}{\partial x^2} + \frac{\partial^2 T}{\partial y^2} \right) + q \]

for the heat source region and

\[ \rho C_p \frac{\partial T}{\partial t} = k \left( \frac{\partial^2 T}{\partial x^2} + \frac{\partial^2 T}{\partial y^2} \right) \quad \text{elsewhere,} \]

where \( T \) is the temperature above the ambient temperature, \( t \) the time, \( \rho \) and \( C_p \) the average density and specific heat of silicon, \( k \) the thermal conductivity of silicon, and \( q \) the rate of heat production per unit time per unit volume when the distance in the z-direction is taken to be unity. The initial condition which \( T(x, y, t) \) must satisfy is

\[ T(x, y, 0) = 0 \quad \text{everywhere} \]

and the boundary conditions are

\[ T(x, y, t) = 0 \quad \text{when} \ y = 0 \]

and

\[ \frac{\delta T}{\delta t} = 0 \quad \text{at all points of the remaining surfaces} \]

where \( \delta T/\delta n \) denotes differentiation in the direction of the outward normal to the surface.

Fig. 3 represents a two-dimensional thermal model of a thermal printing head. Fig. 3(a) and 3(b) shows a conventional planar structure and a V-groove isolation structure, respectively. Although heat sources are randomly in the “on” state, we will consider the case where every other heat source is in the “on” state while the rest are in the “off” state. The primitive cell indicated by the dotted lines in Fig. 3 is considered for the reduction of computation time. The same assumptions as previously stated are also applied to this case.

III. RESULTS AND DISCUSSION

In general, the thermal analysis of a system may be performed by analytic or numerical methods. If the model is simple, it is possible to obtain analytic solutions. If, however,
one must consider the complex chip morphologies or complicated boundary conditions, the problem is usually handled by a computer. In this study, heat flow problems for the two specific examples have been solved numerically using the finite difference method.

First, consider the three kinds of chip morphology in Fig. 2. The values of the parameters are $L_x = 2000$, $L_y = 210$, $h_1 = 400$, and $h_d = 17.5$ (in μm) for Fig. 2(a). These values have been arbitrarily chosen to represent a real situation in integrated circuits, such as a monolithic audio amplifier. In Fig. 2(b) and 2(c), the etch depth $h_d$ is self-determined when we set the oxide opening width $n_1$, due to the property of the V-groove etching. The V-groove etching proceeds in the (100) direction until the front hits the (111) planes, intersecting the (100) plane to make an angle of 54.74° with the surface plane. That is, when we open an oxide pattern line 100 μm wide it will etch 70 μm deep, and other parameters have the same values as in Fig. 2(a). Fig. 4 shows the normalized temperature distributions along the chip surfaces in steady state. $T_{\text{max}}$ denotes the maximum temperature for each structure in Fig. 2 when $q = 7 \times 10^6$ W/cm$^3$. Normalized temperature distributions are independent of $q$ due to homogeneous properties of the heat conduction equations given [2]. Discontinuities of two curves indicate the nonplanar portions on the chip surfaces. Comparing the normalized temperature right outside the heat source region, the V-groove isolation structure has the smallest value and it is about 50 percent of the conventional planar structure. The truncated V-groove structure has a somewhat larger value than the V-groove isolation structure in normalized temperature right outside the heat source region, but it has an important advantage that $T_{\text{max}}$ is much smaller than the other two, i.e., the lowest maximum temperature is obtained in the heat source region with equal rate of heat generation. It may relieve the thermal problem quite efficiently and reduce the cooling cost.

Numerical results of the second example are illustrated in Fig. 5, which shows the normalized temperature distributions along the surface of each primitive cell for a thermal printing head. $T_{\text{max}}$ also represents the maximum temperature of the “on” cell for each structure in Fig. 3 when $q = 7 \times 10^6$ W/cm$^3$. Comparing the normalized temperature of the “off” cell, the V-groove isolation structure has a much lower value, about 60 percent of the planar structure value. This means that V-groove geometry can give smaller thermal crosstalk between “on” and “off” cells and produce better printing quality. V-groove structures require smaller printing energy because the maximum temperature is higher than for planar structures with equal rate of heat production.

In practice, the fabrication of the V-groove and truncated V-groove isolation structures requires (100) orientation silicon wafers anisotropic etched using potassium hydroxide, normal propanol, and deionized water, and one more masking step is needed. During the last few years, great efforts have been concentrated on the V-groove etching process [3] and metallization techniques [4] to gain its acceptance as standard processing technology. For the truncated V-groove structure, a high-quality etching yields a perfectly flat surface with few surface defects [5]. With these developments of V-groove etching technology, it is expected that V-groove structures for thermal isolation will not cause severe problems in manufacturing.

IV. CONCLUSION

The effectiveness of V-grooves for thermal isolation in integrated circuits has been shown by solving the two-dimensional heat flow problem by numerical methods. Numerical results show that the V-groove structure brings about a 50 percent improvement in normalized temperature when compared to the conventional planar structure. Two proposed structures (V-groove isolation and truncated V-groove structure) are shown to be very promising for future development of LSI. It is also shown that the V-groove structure can be used to prepare thermal printing heads with better printing quality and smaller printing energy than the planar structure.

REFERENCES

Beta Measurement and Beta Requirement in I^2L Gates


Abstract—A new approach to beta measurement in the inversely operated I^2L transistor is described, one that avoids arbitrary definitions and terminal-condition specifications. We deactivate the lateral p-n-p by symmetrical biasing so that direct measurement of n-p-n base current becomes possible. Further measurements demonstrate the validity of this approach, and also determine the beta necessary for a desired saturation voltage.

INTRODUCTION

The arrival of I^2L [1], [2], or integrated injection logic, has stimulated considerable modeling effort. In particular, several definitions for the beta of the inversely operated n-p-n transistor have been offered, with accompanying measurement methods, a matter that is not straightforward for the n-p-n has an inaccessible internal node. The methods proposed previously have involved imposing specific conditions on the lateral p-n-p of the merged gate structure [3]–[6]. The beta measurement method offered below treats the p-n-p in a novel way and seeks to answer two questions. First, what value of beta is exhibited by the n-p-n transistor in a given I^2L gate under given operating conditions? Second, what beta value is required in the n-p-n transistor in order to yield a given saturation voltage when sinking current from the subsequent stage?

NEW EXPERIMENTAL APPROACH

In step 1 [Fig. 1(a)], a voltage is applied to the injector terminal and the following parameters are monitored: \( I_0 \), the injector current; \( V_{B2} \), the open-circuit base potential; \( V_{CE} \), the saturated n-p-n collector voltage; and \( I_{C\text{REF}} \), the n-p-n collector current conducted under these conditions. This sets up the initial reference operating condition for the merged switch upon which the subsequent two steps are based.

In step 2, the state of the lateral p-n-p is modified. Separate power supplies are now connected to injector and base, and are adjusted individually until both are equal to the value of \( V_{B2} \) recorded in step 1 [Fig. 1(b)]. Since the forced base potential in step 2 is the same as the monitored open-circuit potential in step 1, the n-p-n collector will still have the same conditions as it did in step 1. This will hold true up to the

Manuscript received November 19, 1980; revised July 23, 1981. This work was supported in part by the National Science Foundation under Grant ENG-77 25007 A01.

J. M. Wisted is with the Microcircuits Operation, Control Data Corporation, Bloomington, MN 55420.

R. M. Warner, Jr., E. M. Murray, and R. P. Jindal are with the Department of Electrical Engineering, University of Minnesota, Minneapolis, MN 55455.