Analysis of Trapped Charges in Dopant-Segregated Schottky Barrier-Embedded FinFET SONOS Devices

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Abstract—The aim of this letter is to analyze the spatial distribution of trapped charges in the type of dopant-segregated Schottky barrier (DSSB)-embedded FinFET SONOS devices used in NAND-type Flash memory. Due to localized programming by carrier injection with extra kinetic energy, the spatial distribution of electrons trapped in an O/N/O layer of a DSSB SONOS device after a short time of programming differs from that in an O/N/O layer of a conventional SONOS device, which results in the degradation of subthreshold slope (SS). Note that the degraded SS recovers as the program time increases. The measured and simulated data confirm that the high speed of the programming is due largely to the localized trapped charges injected from DSSB source/drain junctions.

Index Terms—Dopant-segregated Schottky barrier (DSSB), dopant segregation, FinFET, Flash memory, localized trapping, Schottky barrier, SONOS, subthreshold slope (SS).

I. INTRODUCTION

A SCHOTTKY barrier-type device with dopant segregation at source/drain (S/D) junctions, namely, dopant-segregated Schottky barrier (DSSB) device, is considered a promising candidate for high-performance devices due to its robustness against short-channel effects, low parasitic resistance, and unique hot carrier injection property [1]–[3]. In particular, it reportedly boosts the programming speed when applied to non-volatile memory, which means that the next generation Flash memories will benefit from the aforementioned advantages [4]. The DSSB cell consists of an n-channel Schottky barrier MOSFET in which the S/D junctions are DSSB junctions, i.e., the DSSB junctions are a replacement for the type of diffused S/D p-n junctions in a conventional SONOS device. In addition, a dopant-segregated region is inserted between the metallic silicide and a channel. The excellent programming property that stems from the DSSB nature was demonstrated with a threshold voltage \(V_{th}\) shift of almost 4.5 V under programming conditions of \(V_{PGM} = 12\) V and \(t_{PGM} = 100\) ns for the application of NAND-type Flash memory [4]. By the aid of extra kinetic energy from the sharp band bending at the DSSB junction, tunneling probability near DSSB junction can be exponentially increased. Thereby it drives high-speed programming and local trapping in a short programming time. The spatial distribution of injected electrons in the DSSB device is therefore expected to differ significantly from that in a conventional SONOS device, which utilizes the Fowler–Nordheim (FN) tunneling of electrons without extra kinetic energy as a programming mechanism.

In this letter, we characterize the degradation and recovery property of the subthreshold slope (SS) in a DSSB FinFET SONOS device by using a simple and direct measurement technique that enables us to analyze the spatial distribution of electrons trapped in the nitride of an O/N/O layer as similarly conducted in [7] and [8]. A 2-D numerical device simulation (MEDICI) confirms that the characteristics of SS in the DSSB device are primarily due to the localized trapped electrons. It therefore confirms that the fast programming speed of the DSSB device is mainly due to the injected electrons having extra kinetic energy on the edge of the DSSB junction.

II. RESULTS AND DISCUSSION

The DSSB FinFET SONOS device used for this measurement is the same double-gate device as referred to in [4] and [5]. To eliminate all parasitic effects other than the effect of the localized trapped charges and exclude the possibility of any enhancement of vertical electric field by a narrow fin width [6], we chose devices with a long gate length (300 nm) and a wide fin (60 nm) for this characterization so that we could analyze the SS in relation to various programming times.

Fig. 1 shows the subthreshold characteristics for various programming times. The \(V_{th}\) shift even at the programming time of 32 ns is nearly 4 V, resulting from the enhanced vertical and lateral electric field at the DSSB structure as simulated in inset of Fig. 1. It was also observed that the SS is significantly degraded right after the programming operation with a short time of 32 ns, and it gradually recovers as the programming time increases. This behavior reveals that the degradation of the SS is caused not by the hot carrier-induced interface states but by the localized trapping of electrons. A similar degradation of the SS was also reported in an NROM device, which uses channel hot-electron injection at the drain side as a programming operation [7], [8]. Note, however, that the SS tends to deteriorate rather than recover when the programming time is increased in NROM devices.

A simple mechanism of the programming operation is shown in Fig. 2(a). In the case of short programming time, only the electrons injected from the S/D can have a chance of being trapped in the nitride of the O/N/O layer due to the extra kinetic
energy that originates from the elevated electric field at the edge of the DSSB junction as a result of the sharpened energy band. Thus, a large $V_{th}$ shift is possible even at the short programming time. In the case of long programming time, the electrons at the middle of the channel can be tunneled by the FN tunneling process as usual. This different quantity and location of the trapped charges with respect to the programming time produces a unique SS characteristic, that is, the degradation and recovery depend on the programming time. To investigate the origin of the degradation and recovery of the SS characteristic, we compare the simulated data of three different cases. The aim of this simulation is not showing the exact length of trapped region, but demonstrating localized charge trapping by the intrinsic DSSB structure. Therefore, we can conceptually demonstrate the variation of SS by using simulation. It is speculated that the length of trapped region may be less than 50 nm because localized electric field is distributed within the distance of segregated layer. However, the authors assumed the length of locally trapped region to be 50-nm thickness because the value is suitable enough to show the degradation of SS by nonuniform potential distribution. The proper selection of trapped charges and distribution enables the simulated data to be fitted to the measured data iteratively. Each case of (i), (ii), and (iii) in the measurement data of Fig. 1 corresponds, respectively, to the simulated energy band diagram of (i), (ii), and (iii) in Fig. 2(b). For the best fitted data, spatially distribution of trapped charges can be estimated with several assumptions.

1) The electrons injected from DSSB junctions can be dominantly trapped to the edge of nitride layer in a short programming time. In addition, it is supported by numerically simulated data of lateral electric field along channel direction reported in [5].

2) The density of the trapped charges in the middle of the nitride along the channel is to increase with each increment of the program time from case (i) to case (iii) while that in the edge of the nitride is fixed for simplicity.

From this estimation, each corresponding simulated energy band diagram and its SS to show the same $I_{ds}$ value of 100 pA/µm are attained, as shown in the inset of Fig. 2(b). The results show that the potential distribution is much different each other even at the same $I_{ds}$ value. In the case (i), the dominant charges are located near the edge of gate. Thus, the localized highest potential barrier occurs at the same $I_{ds}$ level. The SS is therefore degraded by the fringing field of the trapped charges in a manner similar to the NROM devices in [7] and [8]. However, as the amount of trapped charges in the middle of the nitride layer along the channel increases with a programming time, the SS begins to recover due to the reduced potential barrier height near the edge of gate as shown from case (ii) to case (iii). This recovery phenomenon is clearly different from the conventional SONOS device which utilizes the global injection of electrons. Through a comparison of the measured data and simulated data, we can conclude that the large $V_{th}$ shift and the degradation of the SS at the short programming time (of 32 ns)
the potential barrier to be lowered to the same level of the channel region, and this behavior causes the height of barrier of the tunneling oxide. Moreover, the unwanted electrons injected from the control gate can also be trapped. (b) Subthreshold characteristics of the DSSB FinFET SONOS device for the PMOS case under programmed states with various programming times.

are the result of the dominantly localized electrons that are trapped by the high electric field at the DSSB junctions. Moreover, the recovery of the SS with the programming time can be attributed to the additional injection of electrons in the middle of the channel region, and this behavior causes the height of the potential barrier to be lowered to the same $I_{ds}$ level.

This unique operating principle can also be adapted to a PMOS case, as shown in the schematic of Fig. 3(a). We fabricated the DSSB PMOS device with the O/N/O gate dielectric by using the same structure except for the boron segregation in the DSSB junctions. For a conventional PMOS device, the holes in the channel cannot be trapped in the nitride of the O/N/O layer due to the high-potential barrier of 4.8 eV. The electrons injected from the DSSB junctions can be trapped near the edge of gate in the same manner as the NMOS case, i.e., due to the extra kinetic energy by the sharpened energy band. Note, however, that the inverted holes in the middle of the channel cannot tunnel into the nitride even with a long programming time because of the high-potential barrier of 4.8 eV. The electrons from the control gate can be adversely trapped in the nitride layer because of the relatively low-potential barrier of 3.1 eV. Consequently, as shown in Fig. 3(b), the SS tends to undergo more degradation than recovery when the programming time is lengthened.

III. CONCLUSION

The variations of the SS are reorganized in Fig. 4 for the devices analyzed in this letter. As discussed earlier, only in the NMOS DSSB case were we able to observe that degradation and recovery of the SS depends on the programming time. This dependence provides further evidence of the fact that the sharpened energy band bending induced by the DSSB structure triggers the injection of hot carriers into the nitride at the edge of gate, thereby significantly enhancing the programming speed in the proposed DSSB SONOS device.

REFERENCES


