Cu/SnAg Double Bump Flip Chip Assembly as an Alternative of Solder Flip Chip on Organic Substrates for Fine Pitch Applications

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Abstract

Recently, the need of fine pitch flip chip interconnection has been continuously growing. In spite of this trend, solder flip chip interconnections have reached the limit in fine pitch applications of less than about 150µm pitch, because bump bridging between adjacent solder bumps occur. Therefore, the investigation on the fine pitch flip chip structure and its reliability are being needed. Metal column and solder double layered (=double bump) flip chip structure is one of the candidates for fine pitch applications. Double bump flip chip structure provides three advantages: 1) fine pitch flip chip interconnection less than 150µm due to straight shape of metal column bumps, 2) better thermo-mechanical reliability by changing the height of metal column bumps, and 3) high current-carrying capability due to excellent electrical conductivity of Cu as one of the column bump materials.

In this study, Cu (60µm) / SnAg (20µm) double bump flip chip were investigated as one of the promising fine pitch interconnections. We successfully demonstrated Cu/SnAg double bump flip chip assembly with 100µm pitch on organic PCB substrates without bridged bumps by optimizing the bonding conditions such as bonding temperature profile, bonding force and flux. Assembled Cu/SnAg double bump joints had stable contact resistance of 12~14mΩ.

And then, we studied interfacial reactions and reliability evaluation of Cu/SnAg double bump flip chip assembly. Cu3Sn, Cu6Sn5, Ni3Sn4, (Cu,Ni)6Sn5, and Ag3Sn IMCs were formed at Cu/SnAg double bump joints after the additional reflow and solid-state aging. Excessive IMC growth and the formation of Kirkendall voids can be one of the origins which can deteriorate mechanical and electrical reliability of flip chip joints.

All Cu/SnAg double bumps showed stable contact resistance after 1000 hours 85°C/85%RH test. And, Cu/SnAg double bumps generally maintained their initial contact resistance after high temperature storage test but showed slightly increased resistance at 150°C due to the formation of Kirkendall voids. On the other hand, contact resistance increased after thermal cycling test. After 1002 cycle T/C test, the failure at Si chip and bump interface was observed in corner and edge bumps. However, center bumps still maintained their contact even after 1000 T/C cycles. The main cause of thermal cycling failures was the Al and Ti UBM depletion between Si chip and Cu column bumps.

Introduction

The need of fine pitch flip chip interconnection has been continuously growing [1]. According to ITRS roadmap, the pad pitch of area array flip chip reduces to 130 µm in 2005, and it will be getting smaller up to 100 µm in 2009 [2]. In this trend, solder flip chip interconnections have reached the limit in fine pitch applications of less than 150 µm pitch, because bump bridging between adjacent solder bumps occur frequently. Therefore, the investigation on the fine pitch flip chip structure and its reliability are needed.

Metal column and solder double layered (=double bump) flip chip structure is one of the candidates for fine pitch applications [3-6]. In this paper, double bump flip chip structures, which consist of Cu column bump and a top SnAg solder bump, are proposed for fine pitch flip chip applications. In double bump structures, Cu column bump plays a role of main interconnection bump and SnAg solder bump functions as a joining layer with substrate pads during flip chip assembly.

Cu/SnAg double bump flip chip structure provides three major advantages compared with conventional solder flip chip interconnection. At first, it enables finer pitch flip chip interconnection without bridged bumps due to straight shape of Cu column bumps. Secondly, it can enhance thermal cycling reliability by changing the bump height. Larger bump height is known to be desirable to reduce the thermo-mechanical shear stress applied to the joint in the flip chip interconnection [3-5]. In the Cu/SnAg flip chip structure, the height of Cu column can be easily increased by an electroplating process. High current carrying capability is expected due to excellent electrical conductivity of Cu. Therefore, this structure can be applied for electrical devices requiring high current or high power.

In this paper, we investigated the interfacial reactions and the reliabilities of Cu/SnAg flip chip assembly with 100µm pitch on organic substrates in order to demonstrate fine pitch interconnection using Cu/SnAg double bumps. The further study is in progress on the other two points, the enhancement of thermal cycling reliability using thick Cu column bumps and current-carrying capability.

Experiments

High performance devices such as a graphic memory and
a CPU chipset adapt fine I/O pad pitch about 120~150 µm, and its I/O configuration tends to be concentrated at a chip center. In this study, a typical graphic memory chip design was chosen to fabricate test chips. The size of test chip was 9.8 mm x 11.03 mm. Test chip had mixed I/Os configuration at the middle of a chip and chip corners. Cu/SnAg double bumps at chip corners were dummy bumps which played a role in leveling the chip during flip chip assembly. Test chip had 128 bumps at the middle of a chip and 64 bumps at chip corners.

Test chips were fabricated using several processes as shown in Fig. 1. First of all, 1500Å-thick silicon oxide layer was deposited on an 8 inch silicon wafer by thermal oxidation, and a Ti (100Å)/TiN (20Å) layer was deposited on the silicon oxide layer as a stress buffer layer and an adhesion layer. And then, 1µm-thick Al layer was sputtered and patterned for metal pads and conductor lines. The size of Al pad was 60µm x 60µm, and the pitch was 100µm. 8µm thick passivation layer was coated using the Intervia8021 of Shipley Company and patterned with 40µm diameter opening. Subsequently, TiW (1000Å) was deposited as an adhesion promotion and a diffusion barrier layer, and then Cu (4000Å) was deposited as a seed layer for electroplating on top surface of silicon wafer. And thick photo-resist, was spin-coated, and patterned by photo-lithography processes. PR thickness was 110µm by double coating, and its opening size was 60µm. After thick PR patterning, Cu and SnAg bumps were deposited using an electroplating method. Cu and Sn2.5Ag solder were electroplated at the current density of 3ASD (Ampere/square decimeter = A/dm²) for 90 minutes and at 3.5ASD for 15minutes, respectively. The target heights of electroplated Cu and SnAg bumps were 60µm and 20µm, respectively. After electroplating of Cu/SnAg double bumps, thick PR was stripped. And Cu and TiW seed layers were etched by their etching solutions for 120sec and 250sec, respectively.

Fig. 2 represents the SEM images of Cu/SnAg double bumps. As shown in Fig. 2(b), the bottom diameter of Cu bumps was about 60µm, and the upper diameter of Cu bumps was about 10µm smaller than bottom diameter due to the undercut of Cu during the seed layer etching.

Fig. 3 shows PCB test substrate used in this study. PCB size was 37.5mm (w) x 37.5mm (l) x 1.0mm (t) and metal pads were 18µm-thick Cu with Ni (8µm)/Au (0.03µm) finish. The opening size and the thickness of PCB solder mask were 50µm and 18µm, respectively. The pitch of PCB metal pads was 100µm. In this study, special PCB solder mask material for 100µm pitch applications was used. This material has
been known to be suitable for fine pitch application of opening diameter of 50µm and minimum space of 15µm [7]. In general, the opening size of PCB solder mask is larger than solder bump diameter so that solder can easily contact and react with PCB metal pads. However, in this study, 50µm opening size of PCB solder mask was used because of the processing limit of fine pitch organic substrates. Larger opening size was an advantage in flip chip assembly, but it may induce some processing problems such as solder mask delamination between adjacent metal pads. Therefore, flip chip assembly conditions and the shape of electroplated Cu bumps were very important for flip chip assembly, because the bump diameter was smaller than the opening size of PCB solder mask.

As shown in Fig. 4, PCB Cu conductor lines were designed for electrical continuity measurement. Daisy chain resistance for Cu/SnAg bumps at the middle of chip center can be measured and the contact resistance of a bump at specific position can be detected using a 4-point Kelvin structure. PCBs had totally 19 Kelvin structured groups classified as three measuring groups, 1) at chip center (3 points), 2) at the edge of a chip (8 points), and 3) at chip corners (8 points).

Flip chip assembly process parameters such as bonding temperature profile, bonding force, and fluxes were optimized in order to assemble flip chip on PCB substrates. A test chip was placed on a chip tool, and a PCB was placed on a heated stage. After alignment process, each temperature was separately controlled by a chip tool heater and a stage heater. In this method, peak temperature of test chip was 280°C, and that of PCB substrate was 120°C. After flip chip assembly, an underfill material was dispensed at 100°C and cured at 170°C for 1 hour. Underfill material includes silica filler of 55%. It has glass transition temperature (Tg) of 120°C, CTE below Tg is 28ppm/°C and CTE above Tg is 100ppm/°C.

To investigate the interfacial reactions of flip chip joints of Cu column/SnAg solder/electroless Ni pad, flip chip samples were reflowed from 1 to 5 times at 250°C and 280°C and aged until 2000 hours at 125°C and 150°C. To clearly observe IMCs at interfaces, SnAg solder was etched away in the mixed solution of methanol, hydrochloric acid and nitric acid. In addition, the contact resistance changes were measured after additional reflow and aging treatments.

For the reliability evaluation of Cu/SnAg double bump flip chip assembly, three reliability tests, 85°C/85%RH (1000 hours), high temperature storage (125°C and 150°C, 2000 hours), and thermal cycling (-55°C, 15minutes ~ +125°C, 15minutes, 1000 cycles) tests were performed. After reliability tests, the contact resistance changes and the failure analysis were performed using by SEM and SAM.

Results and Discussion

1. Cu/SnAg double bump flip chip assembly and interfacial reactions

Fig 5 (a) and (b) represents cross-sectional SEM images of well-assembled Cu/SnAg double bump flip chip. As shown in these figures, SnAg solder bumps were well wetted with PCB Ni/Au pads and the sidewall of Cu bumps. To investigate the existence of underfill voids and bridged bumps inside flip chip samples, SAM analysis was performed. SAM image of Fig. 6 (a) shows that underfill voids were not trapped between chips and PCBs. And Fig. 6 (b) and Fig. 5 (a) presents that no bridged bumps occurred in these flip chip samples. These results demonstrate that Cu/SnAg double bump flip chip structure can solve the bump bridging problem frequently occurred in solder flip chip assembly with less than 150µm pitch. All flip chip assembled samples showed daisy chain resistance of about 8.4Ω. Bump contact resistances of Cu/SnAg double bumps were measured about 12~14mΩ regardless of bump positions as shown in Fig. 7.

![Fig. 5 (a) Cross-sectional image of Cu/SnAg double bump flip chip assembly (b) individual assembled bump image](image1)

![Fig. 6 SAM image of the inside of Cu/SnAg flip chip assembly: No underfill voids and no bridged bumps](image2)

![Fig. 7 Contact resistance of Cu/SnAg double bumps at various bump positions](image3)

The interfacial reactions of Cu column/SnAg solder/ electroless Ni pad are important to evaluate thermal reliability of flip chip assembly. Since Cu/SnAg flip chip assembly has smaller amount of solder bumps compared with conventional solder flip chip, its interfacial reactions show different behavior in terms of the growth of intermetallic compounds and the consumption of solder bumps.
Fig. 8 Cross-sectional images of Cu/SnAg double bump after the number of the additional reflows at 250°C (a) As-assembled, (b) 1, (c) 2, (d) 3, (e) 4, and (f) 5 reflows

Fig. 9 Cross-sectional images of Cu/SnAg double bump after the number of the additional reflows at 280°C (a) As-assembled, (b) 1, (c) 2, (d) 3, (e) 4, and (f) 5 reflows

Fig. 8 and Fig. 9 show the cross-sectional SEM images after additional reflow at 250°C and 280°C, respectively. After the additional reflow, several IMC phases were formed at Cu column/SnAg solder and SnAg solder/ electroless Ni interface. Scallop-like Cu-Sn IMCs were formed at the Cu column side of a chip, and needle-like Ni-Sn IMCs and scallop-like Cu-Ni-Sn IMCs were formed at the PCB side. These IMCs were identified as Cu₆Sn₅, Ni₃Sn₄, and (Cu, Ni)₆Sn₅ by EDS (Energy Dispersive Spectroscopy) analysis. IMC growth rate was proportional to the number of reflow times and reflow temperatures. Cu₆Sn₅ IMCs at the Cu column side grew up to about 5~7µm thickness after five reflows. Needle-like Ni₃Sn₄ IMCs were changed into scallop-like (Cu, Ni)₆Sn₅ IMCs as the number of reflow increased as shown in Fig. 10. During the solder reflow, some IMCs were spalled into SnAg solder. Abnormal Ag₃Sn IMCs and large Cu₆Sn₅ IMCs were observed in SnAg solder. IMC spalling and excessive IMC formation at interfaces can lower the mechanical reliability of Cu/SnAg double bump joints. However, the daisy chain and bump contact resistance was almost same regardless of reflow times as shown in Fig. 11.

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Fig. 10 IMC growth and spalling after 250°C reflow (a) 1, (b) 3, and (c) 5 reflows

Fig. 11 Contact resistance changes at the various additional reflows at 250°C.
Solid-state interfacial reactions were also investigated after aging treatment representing the high temperature storage test of JESD22-A103C of JEDEC standard [8]. Fig. 12 and Fig. 13 represent the cross-sectional images after solid-state aging at 125°C and 150°C. During the test, thick Cu-Sn IMCs grew at Cu/SnAg interface. Total thickness of Cu-Sn IMCs reached about 10µm after 2000 hours aging at 150°C. Scallop-like Cu₆Sn₅ IMC (η) was formed at the interface for the first time. And then Cu₃Sn IMC (ε), darker layer than Cu₆Sn₅ IMC, was formed between Cu₆Sn₅ IMC and Cu column interface. At this time, Cu₆Sn₅ IMCs grew as aging time increased, and Sn atoms were diffused into Cu column/Cu₆Sn₅ IMC interface through channel between Cu₆Sn₅ IMCs [9]. Therefore, Cu₆Sn₅ IMCs were transformed to Cu-rich phase, Cu₃Sn IMCs.

\[
\text{Cu}_6\text{Sn}_5 \rightarrow 2\text{Cu}_3\text{Sn} + 3\text{Sn}
\]

As shown in Fig. 12 and Fig. 13, many Kirkendall voids were observed in Cu₆Sn₅ IMC layer. At 150°C, the size of voids was larger than 125°C, and they were linked each other. It was considered that the formation of Kirkendall voids affected the decrease of contact resistance, because it reduced the contact area of Cu and IMC interface. It resulted from the difference of diffusion rates of Cu and Sn. To form Cu₃Sn IMC, Cu atoms were supplied enough at Cu/Cu₆Sn₅ interface, while Sn atoms had to be diffused across Cu₆Sn₅ IMCs. At this time, 9 Cu atoms needed to form 3 Cu₃Sn IMCs but only 3 Sn atoms needed [9, 10]. Therefore, two vacancies would be formed for one Cu₃Sn IMC.

IMC formation at the PCB side showed the different behavior during reflowing. At 125°C, IMCs were hardly observed on electroless Ni pads except for very thin Ni₃Sn₄ and Cu-Ni-Sn-Au IMCs. However, scallop-like (Cu, Ni)₆Sn₅ IMCs were formed at 150°C, and grew as aging time increased. While the difference of the growth rate was not significant between Cu₆Sn₅ IMCs at Cu/SnAg interface and (Cu, Ni)₆Sn₅ IMCs at SnAg/electroless Ni interface during additional reflows. However, large difference was observed during solid-state aging. Until 500 hours aging, Cu₆Sn₅ phase was main IMCs in the flip chip joints, and then the growth of (Cu, Ni)₆Sn₅ IMCs increased since after 750 hours at 150°C. These differences of IMC growth rate between Cu/SnAg and SnAg/Ni interfaces resulted from the diffusion coefficients of Cu and Ni into liquid and solid Sn. At 287°C, Cu and Ni had similar diffusion coefficient into liquid Sn. However, the diffusion coefficient of Cu into solid Sn is about fifty times higher than that of Ni into solid Sn at 150°C [11, 12]. It is expected that the formation of Kirkendall voids at Cu/SnAg interface and excessive IMC growth in solid-state aging will deteriorate the mechanical strength as well as the electrical contact resistance of flip chip joints.

2. Reliability evaluation of Cu/SnAg double bump flip chip assembly

To evaluate the reliability of Cu/SnAg double bump flip chip assembly, 85°C/85%RH, high temperature storage, and thermal cycling tests were performed. In these tests, dummy bumps at chip corners were not considered in the cumulative distribution of contact resistance because they were not
active I/O bumps even for real memory devices with similar I/O configuration.

![Fig. 14](image1.png)

**Fig. 14** 85°C/85%RH reliability test results of Cu/SnAg double bump flip chip assembly (a) Cumulative distribution and (b) Bump position dependency

![Fig. 15](image2.png)

**Fig. 15** High temperature storage test result of Cu/SnAg double bump flip chip assembly (a) at 125°C and (b) at 150°C

![Fig. 16](image3.png)

**Fig. 16** Thermal cycling test results of Cu/SnAg double bump flip chip assembly (a) cumulative distribution and (b) the ratio of contact resistance of bumps over 100mΩ at various bump positions

Fig. 14 (a) and (b) show 85°C/85%RH reliability test results. All Cu/SnAg double bumps showed stable 85°C/85%RH reliability up to 1000 hours even for dummy bumps at chip corners. After 85°C/85%RH test, Cu-Sn and Ni-Sn IMCs were formed at Cu/SnAg and SnAg/Ni interface, respectively. However, no delamination or cracks were observed and there were no contact resistance changes after 1000 hours test.

Fig. 15 (a) and (b) show high temperature storage test (HTST) results at 125°C and 150°C, respectively. At 125°C, there was no contact resistance change after 2000 hours test. On the other hand, the contact resistances of some Cu/SnAg double bumps slightly increased at 150°C and one of them was electrically opened.

![Image](image4.png)

**Fig. 17** SAM C-scan images of Cu/SnAg double bump flip chip assembly after reliability tests (a) 85°C/85%RH, 1000 hours and (b) Thermal cycling test, 1000 cycles

The further observation of Fig. 18 shows the bump failure mode after T/C test. For the corner bumps, Al/TiW UBMs remained between Si chip and Cu bumps. However, UBMs between Si chip and Cu bumps were depleted after 1000 T/C cycles as shown in Fig. 18 (d) and (e). This result well supported SAM results of Fig. 17. EPMA mapping results of Fig. 19 show the failure mechanism of Cu/SnAg double bump flip chip assembly during thermal cycling. As

![Image](image5.png)

**Fig. 17** SAM C-scan images of Cu/SnAg double bump flip chip assembly after reliability tests (a) 85°C/85%RH, 1000 hours and (b) Thermal cycling test, 1000 cycles

Fig. 16 (a) presents the cumulative distribution of failure rate after thermal cycling test at -55°C (15min) ~ +125°C (15min). Cu/SnAg double bump flip chip assembly had no increase of contact resistance until 407 cycles. However, bump contact resistance increased after 407 cycles and about of 35% Cu/SnAg double bumps had contact resistance larger than 100mΩ after 1000 cycles. Fig. 16 (b) shows the position dependency of bump contact resistance changes after the thermal cycling test. As the distance from chip center increased, contact resistance increased faster. It was considered that larger shear stress acted on the outmost bump joints during thermal cycling [13, 14].

For the failure analysis after thermal cycling test, we performed SAM analysis and cross-sectioned SEM observation. Fig. 17 (a) and (b) present SAM C-scan images after 85°C/85%RH test of 1000 hours and thermal cycling of 1002 cycles, respectively. After 1000 hours 85°C/85%RH test, all bumps had black color. It means that no delamination occurred at bump interface. On the other hand, after 1002 cycle T/C test, the delamination at Si chip and bump interface, presented as white color in SAM images, was observed in corner and edge bumps. However, center bumps still maintained their contact even after 1002 T/C cycles. Contact resistance measurement results of Fig. 15 (b) and Fig. 16 (b) as bump position were well agreed with these SAM images.
shown in Fig. 19, Al and Ti UBM between a Si chip and a Cu column bump was squeezed out. And then, the concentration of Al was higher at interface between Intervia passivation layer and Si chip than at Cu column and Si interface. And, Ti atoms were newly detected at the interface of passivation layer and Si chip. As shown in Fig. 19 (a), since TiW layer was deposited by sputtering after passivation opening process, Ti did not exist at the interface between passivation layer and Al pad on Si chip. It can be explained that the change of Al concentration and the detection of Ti towards the outside from the center of a bump resulted from the friction by cyclic shear force during thermal cycling [15]. The one of the important observations was that the failure by shear stress did not occurred around SnAg solder even though ductile solder bumps were formed as the minimized volume. Therefore, it is expected that higher Cu column bump can enhance the compliance between Si chip and organic substrates during thermal cycling.

![Image](image1.png)

Fig. 18 Thermal cycling failure of Cu/SnAg double bump flip chip assembly (a) SAM image, Cross-sectional image of A position (center bumps) (b) x2000, (c) x10000, Cross-sectional image of B position (corner bumps) (d) x2000, and (e) x10000

Thermal cycling reliability of flip chip assembly depends not only on bump materials and UBM system but also on chip size, bump height, the number of I/Os, I/O configuration, and so on [16]. Therefore, studies on the effects of Cu column bump height and I/O configuration are needed to further enhance the thermal cycling reliability of Cu/SnAg double bump flip chip assembly.

![Image](image2.png)

Fig. 19 EPMA mapping results of Cu/SnAg double joints after thermal cycling (a) Schematic illustration of Cu/SnAg double bump, (b) SEM image of Si chip/Al pad/Cu column interface of corner bumps after 1002 thermal cycles, element mapping results: (c) Al, (d) Ti, (e) Cu, and (f) Si mapping

**Conclusion**

In this paper, Cu/SnAg double bump flip chip assembly on organic PCB substrates was as an alternative of conventional solder flip chip for fine pitch applications. Test chip with Cu (60µm) / SnAg (20µm) double bumps and 100µm pitch was assembled on organic substrates without bridged bumps between adjacent bumps. The contact resistance showed about 12~14mΩ.

To investigate interfacial reactions related to the thermal reliability of Cu/SnAg double bump flip chip assembly, additional reflows and solid-state aging were performed. Cu3Sn, Cu6Sn5, Ni3Sn4, (Cu,Ni)6Sn5, and Ag3Sn IMCs were formed at Cu/SnAg double bump joints after the additional reflow and solid-state aging. Excessive IMC growth and the formation of Kirkendall voids can be one of the origins which can deteriorate mechanical and electrical reliability of flip chip joints.

Finally, 85°C/85%RH, high temperature storage, and thermal cycling tests were performed. All Cu/SnAg double bumps showed stable contact resistance after 1000 hours 85°C/85%RH test. And, Cu/SnAg double bumps generally maintained their initial contact resistance after high temperature storage test but showed slightly increased resistance at 150°C due to the formation of Kirkendall voids.
On the other hand, contact resistance increased after thermal cycling test. As the distance from chip center increased, contact resistance increased faster due to larger shear stress acted on the outmost bump joints during thermal cycling. After 1002 cycle T/C test, the failure at Si chip and bump interface was observed in corner and edge bumps. However, center bumps still maintained their contact even after 1000 T/C cycles. In addition, Al and Ti UBMs between Si chip and Cu column bump were squeezed out due to the friction by cyclic shear force during thermal cycling.

As a conclusion, Cu/SnAg double bump flip chip assembly on organic PCB substrates was successfully demonstrated for 100µm fine pitch flip chip interconnections. To apply Cu/SnAg double bump structure to electrical devices, further studies should be investigated not only on fine pitch interconnection but also on the effect of Cu column bump height for the enhancement of thermal-cycling reliability and the electromigration for high current-carrying capability.

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