Wafer Level Package using Pre-Applied Anisotropic Conductive Films (ACFs) for Flip-Chip Interconnections

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Abstract
Recently, wafer level package (WLP) has become one of the promising packaging technologies due to its advantages such as fewer processing steps, lower cost, and enhanced device performance compared to single chip packages. Many developments on new WLP design, material and process have been accomplished according to the electrical, mechanical performance and reliability requirement of the devices to be packaged. For the lower cost, higher performance and environmentally green packaging process, anisotropic conductive films (ACFs) flip chip assembly has been widely used such as ultra-fine pitch flat panel display (FPD) and general semiconductor packaging applications. However, there has been no previous attempt using on WLP.

In this study, wafer level packages using pre-applied ACFs on a wafer for flip-chip interconnections have been investigated, and the effect of process parameters on the ACF wafer level package performance were investigated. After ACF lamination on an Au stud bumped wafer, and subsequent singulation, and singulated chips were flip-chip assembled on an organic substrate using a thermo-compression bonding method. Au stud bumps were well assembled on Ni/Au pads of organic substrates. And ACF joints between Au stud bumps and substrate pads showed stable bump contact resistance of 8~9mΩ per a bump.

As a summary, new wafer level package method using pre-applied anisotropic conductive films was successively demonstrated for flip chip interconnections. As a result, the newly developed WLP using pre-applied ACFs can be widely used for many non-solder flip chip assembly applications.

Introduction
Wafer level package (WLP) is defined as a package which its interconnection is fabricated on a wafer level prior to chip dicing. Wafer level package merges the front-end semiconductor processing and back-end packaging process together, and it is distinguished from conventional single chip package (SCP) that is accomplished by two clear chip fabrications and packaging. [1, 2]

Therefore, wafer level package has many advantages. Because all processing steps are performed at a wafer level resulting in reduced processing cost. And testing cost can be also saved, because testing for wafer level package can be performed once in a form of known good package (KGP). Wafer level package is truly a chip size package (CSP), which its substrate size is the same as a chip size. Therefore, wafer level packages are very favorable for further miniaturization of electronic devices. [1-3]

Flip-chip interconnection has been widely used to mount IC chips to substrates. In general, it is divided into two categories, solder flip-chip and non-solder flip-chip according to their interconnection methods. Solder flip-chip interconnection has widely used, and wafer level packages using solder bumps have been already commercialized by many developments of wafer bumping and underfill technologies. [4, 5] However, solder has a drawback of process complexity and higher production cost, because it requires several processes such as solder flux coating, solder bump reflowing, flux cleaning, and underfill dispensing and curing. [6]

Currently, anisotropic conductive films (ACFs) have been widely used at flat panel display (FPD) applications such as liquid crystal display (LCD) and plasma display panel (PDP) in forms of chip-on-board (COB), chip-on-glass (COG), and chip-on-flex (COF), and also at general semiconductor packaging applications. Comparing with solder flip-chip, flip chip using ACF has many advantages such as lower processing temperature, environmentally-friendly processes by fluxless process, lower processing cost and enabling the fine pitch applications. However, in spite of these advantages, there has been no previous attempt using ACFs on wafer level packages.

Fabrication processes of ACF wafer level package
Fig. 1 shows the schematic diagram of fabrication process of wafer level package using pre-applied ACF. Fabrication processes divided into three steps as follows: 1) ACF lamination on a wafer, 2) wafer dicing into an individual chip, and 3) flip chip assembly on an organic substrate.

At the first step, ACF was laminated on a non-solder bumped wafer without voids or bubbles. Au stud bumps were used as non-solder bump materials. At that time, ACF should be maintained at B-stage which was not completely cured, because degree of cure of ACF before flip chip bonding may result in deterioration of bump contact resistance and reliability of flip chip joints. In the next step, an ACF-laminated wafer was diced into an individual chip using a diamond blade dicing saw. Because B-stage ACF is softer than silicon, ACF delamination and silicon chipping can occur during wafer dicing process. Therefore, dicing condition should be optimized to avoid sever ACF delamination. In addition, moisture absorption control was also very important in order to enhance the reliability of flip
chip assembly by reducing the moisture-related failure mechanism. [7] Pre-applied ACF on an Au stud bumped wafer was optimized by changing ACF lamination, wafer dicing, and moisture drying conditions. Drying conditions were determined at the condition of complete removal of absorbed moisture and no additional degree of cure of ACF.

Finally, a singulated ACF-laminated chip was flip-chip assembled on organic substrates using a thermo-compression bonding method. ACF-laminated chip was heated to 180°C and maintained for about 20 seconds at 180°C with applied bonding force of 50N. After flip chip assembly, contact resistance was measured using a Kelvin method, and cross-sectional image of Au stud bump/ACF joints was observed by scanning electron microscope.

**Fig. 1 Schematic diagram of fabrication processes using pre-applied ACFs for flip chip applications**

**Test vehicles**

The Si wafer used in this study had a dimension of 4 inch diameter and 500μm thickness, and contained 36 chips of 9mm x 9mm size with 80 peripheral I/Os. Al I/O size was 120μm x 120μm and its thickness was 1μm. Au stud bumps having 80μm diameter and 60μm height were formed on each Al I/O as shown in Fig. 2. Fig. 3 shows the pattern design of test chip and substrate. The substrate size was 30mm x 30mm. PCB metal pads were made up of 8μm thick Ni/Au on 18μm Cu. It had 12 Kelvin structures in order to evaluate contact resistance of Au stud bump/ACF joints.

**Fig. 2 Au stud bumps of a test chip (60μm height and 80μm diameter)**

**Fig. 3 Test vehicle design: (a) 9mm x 9mm test chip, and (b) 30mm x 30mm PCB substrate having Kelvin structures**

**Material properties of ACF**

The thickness of ACF was about 43μm and they had conducting particles of 5μm diameter. Because ACF experienced thermal history during ACF pre-lamination, moisture drying after wafer dicing, and flip chip bonding, DSC (Differential Scanning Calorimetry) analysis was performed to investigate the curing behavior of ACF during processes. Fig. 4 shows the dynamic scan result. The scan rate was 10°C/min from 30°C to 250°C. From the result, the curing of ACF started from about 107.5°C, the onset temperature of ACF curing peak. Table 1 shows curing times at various curing temperatures calculated by an isothermal scan of DSC.

The coefficient of thermal expansion and glass transition temperature of ACF were measured by TMA (Thermo-mechanical analysis) and DMA (Dynamic mechanical analysis) as shown in Table 2. Young’s modulus of ACF was about 1.1GPa at 20°C, as shown in Fig. 5.

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### Table 1: Curing temperature vs. curing time measured from DSC isothermal scan

<table>
<thead>
<tr>
<th>Temperature</th>
<th>160°C</th>
<th>180°C</th>
<th>200°C</th>
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<tbody>
<tr>
<td>Curing time (sec)</td>
<td>26.6</td>
<td>19.7</td>
<td>16.6</td>
</tr>
</tbody>
</table>

### Table 2: CTE and Tg measured by TMA and DMA

<table>
<thead>
<tr>
<th>α1 (ppm/°C)</th>
<th>α2 (ppm/°C)</th>
<th>Tg (°C)</th>
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<tr>
<td>122</td>
<td>3084</td>
<td>104.5°C</td>
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**ACF lamination and wafer dicing processes**

ACF lamination and wafer dicing were the key processing steps in fabricating wafer level package using pre-applied ACF. At first, in order to optimize ACF lamination conditions, the effects of ACF thickness and lamination pressure were investigated. Single layer ACF with 43µm thickness formed many voids due to relatively lower ACF thickness than bump height, so double layer ACF with 85µm thickness was used. Considering the DSC result of ACF, the lamination temperature was determined as 80°C for 1 minute in order to give sufficient adhesion to a wafer. Voids or bubbles were minimized at higher lamination pressure of 60~80psi. Therefore, ACF was laminated at pressure of 80psi.

After ACF lamination, releasing film on ACF was removed, and then the wafer was diced into individual chips. During the wafer dicing, problems, such as ACF delamination, silicon chipping, and moisture absorption into pre-applied ACF on wafer, can occur. Even though complete ACF delamination and severe silicon chipping did not occur, moisture was absorbed during the wafer dicing process. The weight of absorbed moisture was about 0.7% of initial ACF weight. Moisture absorption can be reduced by process changes. First, the releasing film on ACF was removed after the wafer dicing. Releasing film could prevent direct contact of cooling water on ACF during the dicing process. However, extra processing times were required to remove the releasing film from each chip. Second, drying process was adopted just after the wafer dicing. During drying process, ACF should not be cured mush, and absorbed moisture should be fully removed.

Fig. 6 shows the weight change and degree of cure of ACF during drying procedures. For the removal of absorbed moisture inside ACF, it was determined for ACF-laminated wafer to be dried at 100°C for 20minutes. As a result, absorbed moisture inside ACF was completely removed. Longer drying time and higher drying temperature should be avoided, because they caused the increase in degree of cure of ACF. It was interesting to find out that ACF had less weight after drying that as-received, because initial ACF contained
some moisture and solvent residue. Therefore, drying process after wafer dicing was necessary to completely remove moisture or solvent out from ACF.

By optimizing ACF lamination and wafer dicing processes, ACF-laminated chips with Au stud bumps were successfully demonstrated as shown in Fig. 7. From Fig. 7, few voids were formed after ACF lamination, and no ACF delamination was observed after wafer dicing.

![ACF-laminated chip: (a) Overall view and (b) Magnified view of chip corner (Au stud bumps were formed on Al I/Os)](image)

**Flip-chip assembly using pre-applied ACF**

A singulated ACF-laminated chip was flip-chip assembled on organic substrates using a thermo-compression bonding method. Based on DSC analysis results, flip chip bonding condition was determined. The heating rate on ACF-laminated chip was 2.8°C/sec from 65°C to 180°C and then maintained for 20 seconds at 180°C with applied bonding force of 50N. As a result, B-stage ACF was completely cured during the flip-chip bonding process, and fillets were formed along the chip edge. Au stud bumps were well interconnected on Ni/Au pads of organic substrates, and ACF joints between Au stud bumps and substrate pads showed stable bump contact resistances of 8~9mΩ. Fig. 8 shows flip chip assembly using pre-applied ACF and cross-sectional SEM image of Au stud bump/ACF joints. As shown in Fig. 8 (b), Au stud bumps were directly in contact with PCB Ni/Au pads. It means that non-conductive adhesives (NCAs) as well as ACFs can be also used as interconnection materials for wafer level packages. In addition, electroplated Au bumps and electroless Ni/Au bumps can replace the Au stud bumps.

![Flip chip assembly using ACF WLP, (b) Cross-sectional image of Au stud bump/ACF joints, and (c) ACF fillets formed along the chip edge](image)

**Conclusions**

In this study, wafer level packages using pre-applied ACFs for flip-chip interconnections have been developed, and the effect of process parameters on the package performance were investigated. For the WLP process using pre-applied ACF, Au stud bumped Si wafers and conventional ACFs for flip chip assembly were prepared. The newly developed WLP process using pre-applied ACF consists of three simple steps; ACF lamination on Au stud bumped wafer, wafer dicing, and flip chip assembly. In order to demonstrate wafer level package using pre-applied ACF, ACF lamination and wafer dicing condition were optimized by considering processing issues such as void formation, ACF delamination, silicon chipping, moisture absorption and so on. As a result, new wafer level package method using pre-applied anisotropic conductive films was successfully demonstrated for flip chip interconnections. As a result, the newly developed WLP using
pre-applied ACF can be widely used for many non-solder flip chip assembly applications.

References