Development of Three-Dimensional Memory Die Stack Packages Using Polymer Insulated Sidewall Technique

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Abstract—A newly designed three dimensional (3-D) memory die stack package has been established, and the prototype of the 3-D package using mechanical dies has been successfully demonstrated. Fabrication processes of the 3-D package consist of 1) wafer cutting into die segments, 2) die passivation including sidewall insulation, 3) via opening on the original I/O pads, 4) I/O redistribution from center pads to sidewall, 5) bare die stacking using polymer adhesive, 6) sidewall interconnection, and 7) solder balls attachment.

There are several significant improvements in this new 3-D package design compared with the current 3-D package concept. The unique feature of this newly developed package is the sidewall insulation of dies prior to the I/O redistribution of dies, which produces 1) better chip-to-wafer yields and 2) significant process simplification during subsequent fabrication steps. According to this design, 100% of die yields on a conventional wafer design can be obtained without any neighboring die losses which usually occur during the I/O redistribution processes of conventional 3-D package design. Furthermore, the new 3-D package design can simplify the following processes such as I/O redistribution, sidewall insulation, sidewall interconnection, and package formation. It is proven that the mechanical integrity of the prototype 3-D stacked package meets requirements of the JEDEC Level III and 85°C/85% test.

Index Terms—Bare die stacking, reliability tests, sidewall insulation, three-dimensional packaging, vertical interconnection.

I. INTRODUCTION

As the complexity of electronic systems for portable electronic, aerospace, and military applications increases, more demands are requested on low power, light weight, and compact packaging technologies. In order to meet these demands, three-dimensional (3-D) packaging technology, first introduced by IBM in the 1970’s, is now emerging as a breakthrough in overcoming the limit of two-dimensional (2-D) packages. There is a dramatic improvement in compactness resulting in a lower overall interconnection length, lower parasitic properties and thereby reduced system power consumption [1]–[3]. When considering silicon efficiency, the ratio of total chip area to the footprint area of package, 20–90% of silicon efficiency can be obtained from the current MCM packages. However, 3-D technology can provide more than 100% silicon efficiency compared to other 2-D packaging technologies. Although 3-D packaging technology can offer remarkable advantages, there are still a few hindrances for this technology to be extensively applied. A major drawback of the full implementation of 3-D packaging is the high packaging cost mainly due to process complexity.

There are three conventional 3-D packaging technologies such as package stack, module stack, and bare die stack packages according to what is stacked. Among these, bare die stack package is the most advanced type with respect to compactness, integration density, and electrical performance. Currently, it has been reported that IBM, Irvine Sensors, Fujitsu, TI, and Cubic Memory are working on the area of bare die stacking technology. The major differences between these technologies occur at the sidewall insulation and interconnection method, required for power, ground, and signals routing at the sidewall of stacked packages [4]. IBM-Irvine Sensors’ sidewall interconnection technique requires silicon etching, polymer dielectric injection, and sidewall grinding after bare die stacking for the sake of sidewall insulation [5], [6]. In contrast, the Cubic Memory’s bare die stacking technology interconnects I/O’s at the sidewall using conductive paste technique after bare die stacking [7]. Each method has its own limit in terms of package density, chip-to-wafer yield, and process complexity.

Therefore, there is a need for a simpler and more cost-effective 3-D packaging method than current 3-D bare die stacking technologies. In this study, newly developed 3-D memory die stack package design, material systems, and the process flow will be discussed, and the reliability of the package will be evaluated.

II. FABRICATION

The fabrication starts from sidewall insulation of the wafer segments containing about 10 dies. I/O pads originally located at the center line of the memory chip are redistributed to the sidewall insulating layer. I/O redistributed dies are stacked together, and then interconnected at the polymer insulated sidewall of the stacked module. Finally, solder balls are attached on the sidewall metal pad for the next level assembly.

The material systems selected for the 3-D package fabrication are 525 μm thick silicon, 25 μm thick Kapton-HN film as a die passivation layer. A thermoplastic adhesive, named TPA 1 for convenience, is coated on the Kapton film as an adhesive.
Fig. 1. Sidewall insulated wafer segments (top) top surface and (bottom) cross-sectional view.

Another thermoplastic adhesive is also chosen as a sidewall insulating layer, called TPA 2. And the other thermoplastic adhesive, TPA 3, is used to stack dies. Al and combination of Ti/Cu metallization are adapted as conducting lines for the I/O redistribution and the sidewall interconnection, respectively. Detailed fabrication processes are as follows.

A. Sidewall Insulation

The unique feature of this new 3-D packaging technology is that the sidewall insulation is performed prior to the I/O redistribution. This process results in improved fabrication yield and simplified processing steps. As the first step of sidewall insulation, the fully processed wafer is diced into several wafer segments, containing one or two rows of chips. After the wafer segments and TPA 2 strips as thick as the wafer are placed alternately on the TPA 1 coated Kapton film, another TPA 1 coated Kapton film is placed onto the the wafer segments and TPA 2 strips as upside down manner. Heat and pressure are applied in order to reflow TPA 1 and TPA 2. When samples are cooled down, TPA 1 and TPA 2 are solidified providing strong adhesion with the wafer segment, because they are thermoplastic polymers. Fig. 1(top) and (bottom) are optical micrographs showing top surface and cross-sectional view of sidewall insulated wafer segments, respectively.

B. I/O Redistribution

I/O redistribution is performed after the sidewall insulating layer formation. Typical memory chips having center I/O pads can not be directly used for bare die stack package fabrication because electrical interconnection between stacked dies should be performed at the sidewall of the stack structure. Therefore, I/O redistribution to the sidewall is required before die stacking process. The I/O redistribution consists of via opening, metallization, and patterning. Vias were opened on original I/O pads through TPA 1 layer and Kapton passivation film using O₂ or O₂/CF₄ gas mixture reactive ion etching (RIE). Fig. 2 shows the sloped via formed by O₂ RIE. Al metallization and patterning was performed to interconnect original I/O pads to sidewall of insulated die. Because redistributed I/O pads are connected to the sidewall interconnecting metal line as T-joint connection, more than 1 μm thickness of I/O redistributed metal pad is recommended. The redistributed I/O pads on the sidewall insulating layer are shown in Fig. 3(a) and (b).

C. Die Stacking

The next step is to stack the I/O redistributed bare dies along the Z-axis. Wafer segments are singulated into unit dies using a diamond cutting saw. Four dies are stacked together to form a module. Thermoplastic adhesive (TPA 3) used for die stacking process provides a good adhesion strength, leading to a high mechanical integrity of the stacked module. Non-uniform coating of the adhesive can cause several voids or gaps between the stacked dies, resulting in a discontinuous metallization across the dies upon the sidewall interconnection. Therefore, the TPA 3 adhesive coated on the die surface should be reflowed and completely planarized during die stacking process with applied pressure and temperature over Tg of the TPA 3. Fig. 4(a) shows the bare die stacked module using TPA 3. Every chip in the stacked module is well aligned to one another as shown in Fig. 4(b). And Fig. 4(c) also shows no significant void or gap is observed between dies using the TPA 3 thermoplastic adhesive.
Fig. 3. Optical micrographs of (a) I/O redistributed wafer segment and (b) magnified view of the redistributed I/O pads on the sidewall insulating layer.

D. Sidewall Interconnection

After die stacking, sidewall interconnection is carried out interconnect individual sidewall insulated dies. Power, ground, and signals are routed on the sidewall of the stacked module. As mentioned earlier, the sidewall interconnection can be carried out just after the die stacking process because the redistributed I/O's exposed at the sidewall of the stacked module are already electrically isolated by the TPA 1 and TPA 2 polymers. This is the most unique feature of the newly developed 3-D package compared with other existing 3-D die stack packages. Ti/Cu combination metal is used as the sidewall interconnecting metal line and also as the under bump metallurgy (UBM) of eutectic Pb/Sn solder balls, will be attached the later step. It was reported that Ti/5 μm Cu UBM system maintains good adhesion with eutectic Pb/Sn solder ball and long term reliability [8]. Fig. 5 shows the sidewall interconnecting Ti/Cu metal pattern of a 4-die stacked module. Address, ground, power, and some control lines are bussed, but the data lines and other control lines are not bussed. The line width is 100 μm and the pad is 400 μm square.

E. Solder Ball Attachment

The final step of the 3-D package fabrication is to attach solder ball on the sidewall metal pad for the next level packaging assembly. 300 μm diameter eutectic Pb/Sn solder ball is attached to the Ti/Cu metal pad coated with solder flux in an infra-red solder reflowing oven. For a better solder ball registration, a solder mask layer can be applied on the surface. Fig. 6 shows the prototype of the 3-D bare die stack package after whole processes completed.

Fig. 5. Patterned metal line on the sidewall of 4-die stacked module.

Fig. 6. Prototype of the completed 4-bare die stacked module with 300 μm diameter eutectic Pb/Sn solder balls attached to metallized sidewall pads.

III. Unique Features

The newly developed 3-D bare die stack packaging technology has several advantages over conventional 3-D packaging technologies.

A. High Density Package

Current 3-D packaging technologies can be classified into three groups: package stack, module stack, and bare die stack packages. And bare die stack packages are superior to the others in terms of the silicon efficiency and the electrical performance. The 3-D bare die stack package in this study maintains much
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Fig. 7. I/O redistribution method designed by Irvine Sensors [5], [6]. Only one die per segment including six dies can be applicable to 3-D package fabrication.

Fig. 8. I/O redistribution method according to this new 3-D package. All of the dies in the processed wafer can be used for 3-D package fabrication.

smaller size and higher integration density than the other two 3-D packaging technologies or conventional 2-D packaging approaches.

B. Process Simplicity

One of the major drawbacks of the full implementation of 3-D packaging technologies is the high fabrication cost due to the process complexity. Figs. 7 and 8 are schematic illustrations showing the two different approaches for insulating the sidewall and redistributing the original I/O’s to a die edge line according to the Irvine Sensors’ design and this newly developed design, respectively. For Irvine Sensors’ technology the redistributed I/O pads are placed on the neighboring dies before any insulating layer formation process. Therefore, it requires several additional steps, such as silicon etching, polymer dielectric injection, and sidewall planarization to electrically isolate the I/O pads prior to the sidewall interconnection. In contrast, the sidewall insulating layer can be easily formed before I/O redistribution in this new 3-D package design as described before. In addition, the redistributed I/O pads at the sidewall insulating layer are already electrically isolated. Therefore, no additional treatment is required for the sidewall interconnection after bare die stacking, resulting in a much simpler fabrication process compared with the conventional approaches.

C. Better Chip-to-Wafer Yield

Only one chip per segment containing 6 dies can be used for the 3-D package fabrication in accordance with the Irvine Sensors’ technology. This is because redistributed I/O pads are formed on the neighboring dies, as schematically illustrated in Fig. 7. On the other hand, the newly developed 3-D package forms redistributed I/O pads on the sidewall insulating layer. Therefore, all of the chips in the wafer can be utilized to fabricate 3-D package as shown in Fig. 8, resulting in a significant improvement in the die-to-wafer fabrication yield.

IV. RELIABILITY TESTS

JEDEC level III test and high temperature/high humidity (85°C/85%) test were conducted on the prototypes of 3-D bare die stack packages. These reliability tests were performed to verify the selected material systems and the unit process conditions and to prove the structural integrity of the 3-D bare die stack package.

A. JEDEC Level III Test

The test condition of JEDEC level III is 30°C/60%RH/196 h followed by IR reflowing above 183°C for 1.5 min. Optical microscopy observation was employed to examine mechanical failure or degradation after the test. No significant delamination or structural change was found after the JEDEC level III test.

B. High Temperature/High Humidity Test

High temperature/high humidity test of 85°C/85%RH/720 h was used to investigate the mechanical reliability of the packages. It was found that more than 90% of the test samples maintained the mechanical integrity.

V. CONCLUSION

A new design of 3-D bare die stack package with simpler processing steps and better die-to-wafer yields has been established. And a prototype of the 3-D memory die stack package using mechanical dies has been successfully demonstrated. The fabrication processes of the 3-D bare die stack packaging are

1) wafer cutting into die segments;
2) sidewall insulation of dies using polymer lamination;
3) via opening on the original I/O pads;
4) I/O redistribution from center pads to the sidewall insulating layer;
5) die stacking using polymer adhesives;
6) sidewall metallization and patterning;
7) solder balls attachment.

The most unique feature of this newly developed package design is the sidewall insulation prior to the I/O redistribution, which brings about 1) better die-to-wafer yield and 2) significant process simplification in subsequent fabrication steps. By using this new 3-D design, all of dies on a conventional wafer can be utilized for 3-D bare die stack package fabrication without any
neighboring die loss associated with I/O redistribution to sidewall. Furthermore, this design can simplify the following processes such as I/O redistribution, sidewall insulation, sidewall interconnection, and package formation.

The mechanical integrity of prototype 3-D bare die stack packages meets the JEDEC Level III and 85°C/85% test.

REFERENCES


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