1-bit and Multi-bit Envelope Delta-Sigma Modulators for CDMA Polar Transmitters

Woo-Young Kim, Ki-Young Kim, Seung-Tak Ryu, Jae-Kil Jung and Chul Soon Park
Intelligent Radio Engineering Center (IREC), School of Engineering,
Information and Communications University (ICU),
119, Munjiro, Yuseong-gu, Daejeon, 305-732, Korea
parkcs@icu.ac.kr

Introduction

Two key design issues of power amplifiers (PAs) are the linearity and efficiency. Traditional linear PA has good linearity but its poor efficiency has been the major drawback. In order to improve the efficiency of PA, several innovative transmitter architectures have been suggested and implemented using envelope elimination and restoration (EER) [1], bandpass delta-sigma modulator (BPDSM) [2], or envelope delta-sigma modulator (EDSM) [3].

Even though the EER transmitter improves the efficiency by modulating the power supply of PA, AM/AM and AM/PM distortion still remain as the major drawback of this architecture [4]. Ideal BPDSM shows high efficiency and high linearity. But since it requires the sampling frequency to be higher than four times of RF carrier frequency, which results in more than a few GHz sampling, CMOS implementation is hardly possible with current technology.

In contrast, EDSM provides high linearity with a reasonable sampling frequency. Unlike EER, power supply of PA is fixed and thus it is free from AM/AM and AM/PM distortion problems. Compared with BPDSM, EDSM can reduce the sampling frequency drastically down to 100 MHz or below it with proper OSR because EDSM deals with baseband envelope information.

From those advantages mentioned above, EDSM is expected to be the most promising architecture for the next generation polar transmitter application. Nevertheless, real circuit design of EDSM for polar transmitters has rarely been reported so far. This work focused on the EDSM design for CDMA polar transmitters architecture based on the Agilent ADS Ptolemy simulation and the Cadence circuit simulation.

1- bit EDSM for CDMA Polar Transmitters

Fig. 1 shows CDMA polar transmitters using 1-bit EDSM. The performance of the transmitter has been studied using the Agilent ADS Ptolemy simulation. The EDSM in the simulation has a 1-bit second-order architecture with various OSR from 4 to 128. Higher-order EDSM can achieve higher signal-to-noise ratio (SNR), but it makes the whole circuitry complex and guaranteeing the modulator stability becomes difficult. Thus, the second-order architecture has been selected for this work. Fig. 2 shows output spectrum of PA and Fig.3 shows the ACPR versus various OSR of 1-bit second-order EDSM. The simulation result reveals that OSR 32 satisfies the linearity requirements of CDMA IS-95A signal for both 885 kHz offset and 1.98 MHz offset cases.

From the simulation results, the 1-bit second-order EDSM with OSR 32 has been selected and designed using Cadence circuit simulation. Since the bandwidth of the CDMA IS-95A signal is 1.25 MHz, the sampling frequency of EDSM is determined to be 80 MHz by OSR 32. Fig. 4 shows the block diagram of the designed EDSM. It has been designed for the 0.18-μm CMOS technology. The EDSM has been designed with the switched-capacitor (SC)

978-1-4244-2642-3/08/$25.00 ©2008 IEEE

integrators. Fully differential folded-cascode amplifiers have been used for the wide output swing. The performance parameters of the op-amp are summarized in Table 1. From the simulation, the peak SNR of EDSM is 57 dB, and the dynamic range is 60 dB while consuming the static power of 3.6 mW. Fig. 5 shows the output spectrum of the EDSM. The layout of the EDSM is shown in Fig. 6, where the chip size is 1mm x 1mm including bonding pads. Table 2 summarizes the overall EDSM performance.

Multi-bit EDSM for CDMA Polar transmitters

Even though the designed 1-bit EDSM satisfies the design requirements of CDMA polar transmitters, lower OSR is desirable in order to reduce the slew limitation and to reduce the switching power consumption. Furthermore multi-level output power driving is a desirable technique to achieve higher linearity and higher efficiency. Thus, in this Section, authors suggest a possible configuration of a CDMA polar transmitter using multi-bit EDSM .

Fig. 7 shows the output spectrum of PA from the Agilent ADS Ptolemy simulation with various quantization resolution of the second-order EDSM with OSR 32. Fig. 8 shows ACPR simulation versus quantization resolution for OSR 32 and 16 cases. Fig. 8 concludes that a 2-bit second-order EDSM with OSR 16 satisfies the design target of this work.

Now, the problem is how to implement the multi-bit EDSM in the polar transmitter. The authors suggest one possible architecture named the decoded switch control method. Fig. 9 shows the proposed architecture of polar transmitter with the 2-bit EDSM. The 2-bit data from the EDSM output is decoded into a 4-bit data and each bit of the decoder output is connected to the dedicated switch which is connected to its dedicated supply voltages, VDD1, VDD2, VDD3,and VDD4. The supply voltages should have step size for the linear output power. In the case of EDSM outputs for 00, 01, 10,and 11, the PA output drain node will be connected to VDD1, VDD2, VDD3, and VDD4 respectively.

Such various supply levels can possibly be generated using hardware and power efficient DC/DC converters such as the single-inductor-multi-output (SIMO) configured DC/DC converters. When everything is ideal, ACPR is -55 dBc at 885 kHz offset, -60 dBc at 1.98 MHz offset with the proposed multi-bit EDSM. This satisfies the CDMA IS-95A linearity requirements. Fig. 8 shows that 3-bit EDSM or even with higher number of bit EDSM structure can provide even better performance, but due to the expected hardware complexity it doesn't seem to be the best choice.

Conclusion

The 1-bit second-order EDSM with OSR 32 for a CDMA polar transmitter has been designed using Cadence circuit simulation, where the design specifications have been extracted from the Agilent ADS Ptolemy simulation. And multi-bit EDSM is able to reduce the sampling frequency, while providing reduced slew limitation and reduced switching power consumption. This paper proposes one possible architecture with multi-bit EDSM named the decoded switch control method. Multi-level power driving is expected to provide higher linearity and higher efficiency.

Acknowledgements: This work was supported by the Ministry of Education, Science and Technology (MEST)/Korea Science and Engineering Foundation(KOSEF) as the Intelligent Radio Engineering Center (IREC) of Korea under the Science Research Center (SRC)/Engineering Research Center (ERC) Program (No. R11-2005-029-02001-0).

REFERENCE

[1] L. R. Kahn, "Single sideband transmission by envelope elimination and restoration," *Proc. IRE*, vol. 40, pp. 803–806, July 1952.

[2] A. Jayaraman, P. F. Chen, G. Hanington, L. Larson, and P. Asbeck, "Linear high-efficiency microwave power amplifiers using bandpass delta–sigma modulators," *IEEE Microw. Guided Wave Lett.*, vol. 8, no.3, pp. 121–123, Mar. 1998.

[3] Y. Wang, "An improved Kahn Transmitter Architecture Based on Delta-Sigma Modulation, "*Microwave Symposium Digest, 2003 IEEE MTT-S* , Vol.2, pp.1327 -1330 vol.2, June 2003.

[4] Jinsung Choi, "A Delta-Sigma-Digitized Polar RF Transmitter," IEEE Trans. *Microw. Theory Tech*., vol.55, no.12,pp.2679-2690, Dec.2007.

[5] K.Y.Kim, "Parastec Capacitance Optimization of GaAs HBT Class E Power Amplifier for High Efficiency CDMA EER Transmitter," *IEEE RFIC Symposium*, pp.733-736, 2007.

[6] R. Schreier, and G.C. Temes, *Understanding delta-sigma data converters*. IEEE Press, 2005.

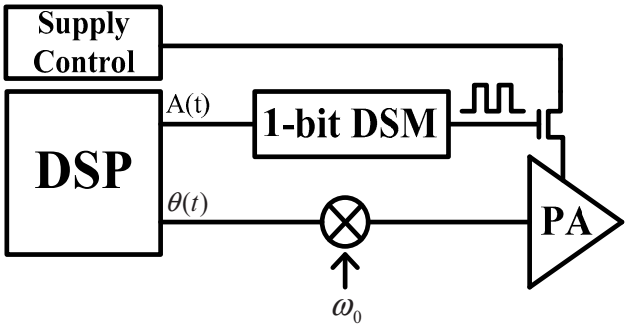

Fig. 1. A CDMA polar transmitter using 1-bit EDSM

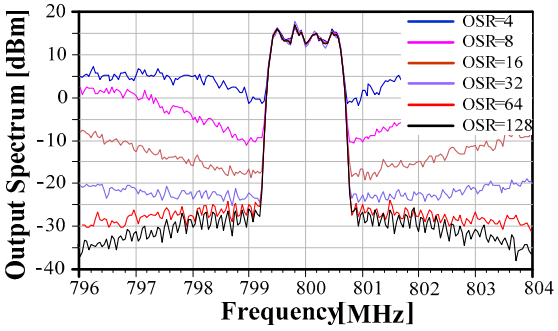

Fig. 2. Output spectrum of PA

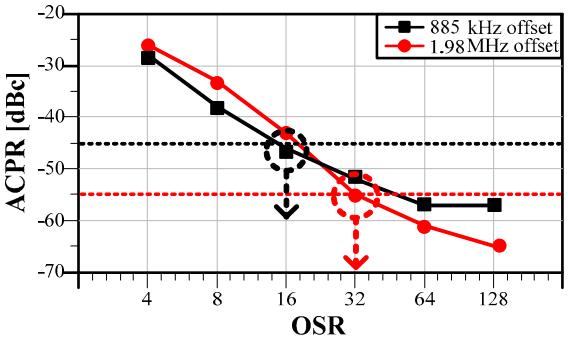

Fig. 3. ACPR versus OSR

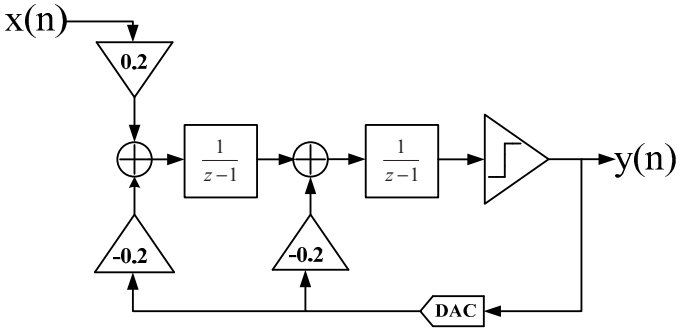

Fig.4 . the block diagram of the designed EDSM

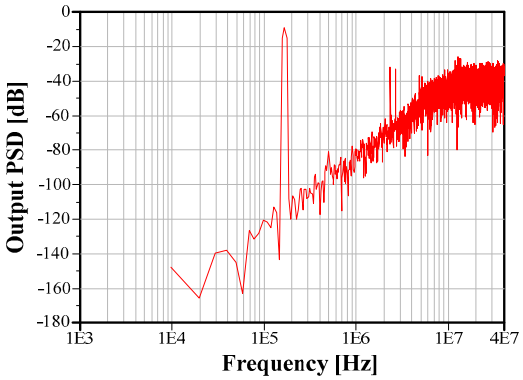

Fig. 5. 1-bit EDSM output spectrum

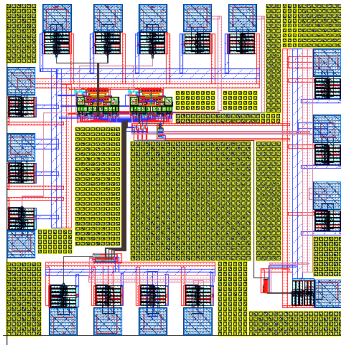

Fig.6. 1-bit EDSM layout

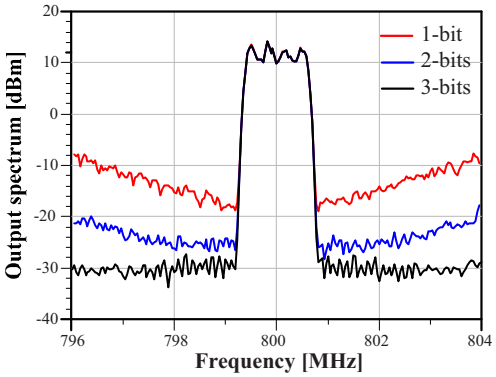

Fig.7. Output spectrum versus bits (OSR=32)

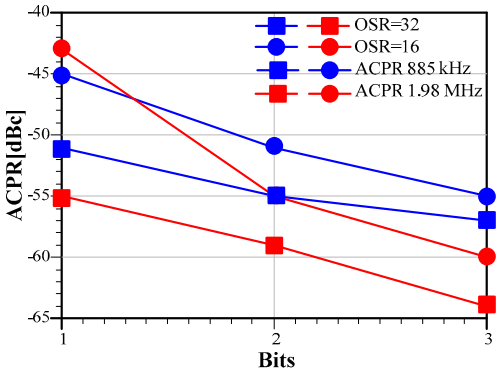

Fig.8. ACPR versus bits

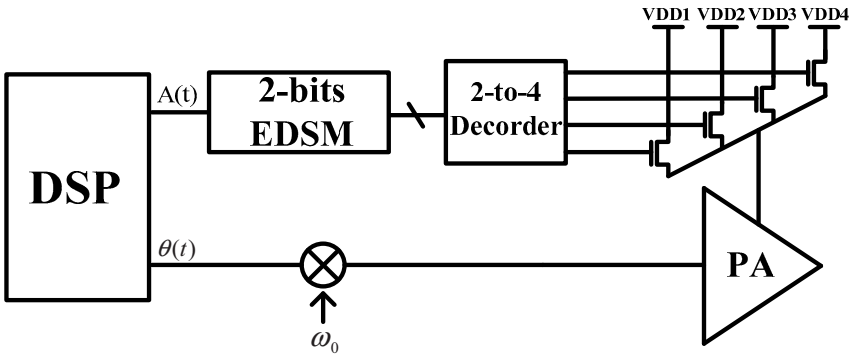

Fig. 9. A CDMA polar transmitter using 2-bit EDSM

Table I
Op-amp parameter

Specification	Op-amp
DC Gain	60 dB
Phase Margin	72°
GBW (CL=0.5p)	520 MHz
Power	1.44-mW

Table II
Performance summary

Specifications	Value
Sampling rate	80 MHz
OSR	32
Signal bandwidth	1.25 MHz
Dynamic Range	60 dB
SNR	57 dB
Active Area	1 mm x 1 mm
Technology	TSMC 0.18um CMOS